AT114A

C²MOS INTEGRATED CIRCUITs

APPLICATIONS

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TO

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INTEGRATEDCIRCUIT

TECHNICAL DATA

TC4000 Series

Product Name	Function
TC4001BP/UBP	QUAD 2-INPUT POSITIVE NOR GATE
TC4002BP	DUAL 4-INPUT POSITIVE NOR GATE
TC4006BP	18-STAGE STATIC SHIFT REGISTER
TC4007UBP	DUAL COMPLEMENTARY PAIR PLUS INVERTER
TC4008BP	4-BIT FULL ADDER
TC4009UBP	HEX INVERTING BUFFER/CONVERTER
TC4010BP	HEX NON-INVERTING BUFFER/CONVERTER
TC4011BP/UBP	QUAD 2-INPUT POSITIVE NAND GATE
TC4012BP	DUAL 4-INPUT POSITIVE NAND GATE
TC4013BP	DUAL "D"-TYPE FLIP FLOP
TC4014BP	8-STAGE STATIC SHIFT REGISTER
TC4015BP	DUAL 4-STAGE STATIC SHIFT REGISTER
TC4016BP	QUAD BILATERAL SWITCH
TC4017BP	DECADE COUNTER/DIVIDER
TC4018BP	PROGRAMMABLE DIVIDE-BY-N COUNTER
TC4019BP	QUAD AND-OR SELECT GATE
TC4020BP	14-STAGE BINARY COUNTER
TC4021BP	8-BIT PARALLEL IN/SERIAL OUT S.R
TC4022BP	DIVIDE BY 8-COUNTER/DIVIDER
TC4023BP	TRIPLE 3-INPUT POSITIVE NAND GATE
TC4024BP	7-STAGE BINARY COUNTER
TC4025BP	TRIPLE 3-INPUT POSITIVE NOR GATE
TC4027BP	DUAL J/K MASTER-SLAVE FLIP FLOP
TC4028BP	BCD TO DECIMAL DECODER
TC4029BP	PRESETTABLE UP/DOWN COUNTER
TC4030BP	QUAD EXCLUSIVE-OR GATE
TC4032BP	TRIPLE POSITIVE SERIAL ADDER
TC4034BP	8-BIT LBIDIRECTIONAL BUS REGISTER
TC4035BP	4-BIT PARALLEL IN/PARALLEL OUT S.R
TC4036BP	4 WORD BY 8 BIT STATIC RAM
TC4038BP	TRIPLE NEGATIVE SERIAL ADDER
TC4039BP	4 WORD BY 8 BIT STATIC RAM
TC4040BP	12-STAGE BINARY COUNTER

TC4000 Series

Product Name	Function
TC4042BP	QUAD "D"-LATCH
TC4043BP	QUAD POSITIVE NOR R/S LATCH
TC4044BP	QUAD POSITIVE NAND R/S LATCH
TC4047BP	ASTABLE/MONOSTABLE MULTIVIBRATOR
TC4049BP	HEX INVERTING BUFFER/CONVERTER
TC4050BP	HEX NON-INVERTING BUFFER/CONVERTER
TC4051BP	SINGLE 8-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER
TC4052BP	DIFFERENTIAL 4-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER
TC4053BP	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER
TC4054BP	4-LINE LC DISPLAY DRIVER
TC4055BP	BCD TO 7-SEGMENT LC DISPLAY DRIVER
TC4056BP	BCD TO 7-SEGMENT LC DISPLAY DRIVER
TC4063BP	4-BIT MAGNITUDE COMPARATOR
TC4066BP	QUAD BILATERAL SWITCH
TC4068BP	8-INPUT POSITIVE NAND GATE
TC4069UBP	HEX INVERTER
TC4071BP	QUAD 2-INPUT POSITIVE OR GATE
TC4072BP	DUAL 4-INPUT POSITIVE OR GATE
TC4073BP	TRIPLE 3-INPUT POSITIVE AND GATE
TC4075BP	TRIPLE 3-INPUT POSITIVE OR GATE
TC4076BP	QUAD "D"-TYPE REGISTER
TC4078BP	8-INPUT POSITIVE NOR GATE
TC4081BP	QUAD 2-INPUT POSITIVE AND GATE
TC4082BP	DUAL 4-INPUT POSITIVE AND GATE
TC4085BP	DUAL 2-WIDE AND OR INVERT GATE
TC4086BP	4-WIDE AND OR INVERT GATE
TC4093BP	QUAD 2-INPUT NAND SCHMITT TRIGGER
TC4094BP	8-STAGE SHIFT AND STORE BUS REGISTER
TC4099BP	8-BIT ADDRESSABLE LATCH
TC40107BP	DUAL 2-INPUT NAND BUFFER/DRIVER
TC40160BP	DECADE COUNTER WITH ASYNCHRONOUS CLEAR
TC40161BP	4-BIT BINARY COUNTER WITH ASYNCHRONOUS CLEAR
TC40162BP	DECADE COUNTER WITH SYNCHRONOUS CLEAR

TC4000 Series

Product Name	Function
TC40163BP	4-BIT BINARY COUNTER WITH SYNCHRONOUS CLEAR
TC40174BP	HEX TYPE D-FLIP FLOP
TC40175BP	QUAD TYPE D-FLIP FLOP
TC40192BP	PRESETTABLE UP/DOWN BCD COUNTER
TC40193BP	PRESETTABLE UP/DOWN 4 BIT BINARY COUNTER

TC4500 Series

Product Name	Function
TC4508BP	DUAL 4-BIT LATCH
TC4510BP	BCD UP/DOWN COUNTER
TC4511BP	BCD TO 7-SEGMENT LATCH/DECODER/DRIVER
TC4512BP	8-CHANNEL DATA SELECTOR
TC4514BP	4-BIT LATCH/4-TO-16 LINE DECODER
TC4515BP	4-BIT LATCH/4-TO-16 LINE DECODER
TC4516BP	BINARY UP/DOWN COUNTER
TC4518BP	DUAL BCD UP COUNTER
TC4520BP	DUAL BINARY COUNTER
TC4521BP	24-STAGE FREQUENCY DIVIDER
TC4522BP	PROGRAMMABLE DIVIDE-BY-N 4-BIT BCD COUNTER
TC4526BP	PROGRAMMABLE DIVIDE-BY-N 4-BIT BINARY COUNTER
TC4527BP	BCD RATE MULTIPLIER
TC4528BP	DUAL MONOSTABLE MULTIVIBRATOR
TC4531BP	12-BIT PARITY TREE
TC4532BP	8-BIT PRIORITY ENCODER
TC4539BP	DUAL 4-CHANNEL MULTIPLEXER
TC4543BP	BCD TO 7-SEGMENT LATCH/DECODER/DRIVER
TC4555BP	DUAL 1 OF 4 DECODER (POSITIVE)
TC4556BP	DUAL 1 OF 4 DECODER (NEGATIVE)
TC4560BP	N BCD ADDER
TC4561BP	9'S COMPLEMENTER
TC4572BP	HEX GATE 4-INVERTERS PLUS 2-INPUT NOR GATE PLUS 2-INPUT NAND GATE
TC4583BP	DUAL SCHMITT TRIGGER
TC4585BP	4-BIT MAGNITUDE COMPARATOR

TC5000 Series

Product Name	Function
TC5001P	4-DIGIT DECADE COUNTER
TC5002BP	BCD TO 7-SEGMENT DECODER/DRIVER
TC5003P	TV SYNC GENERATOR
TC5010P	4-DIGIT UP/DOWN COUNTER WITH TIMER
TC5012BP	3-STATE NON-INVERTING BUFFER
TC-5018P	4-STAGE BINARY COUNTER WITH R.C./OSC
TC5020BP	HEX LOW TO HIGH TRANSLATOR
TC5022BP	BCD TO 7-SEGMENT DECODER/DRIVER
TC5023BP	16 CHANNEL MULTIPLEXER
TC5024BP	QUAD 3-STATE BUS BUFFER ("L" LEVEL)
TC5025BP	QUAD 3-STATE BUS BUFFER ("H" LEVEL)
TC5026BP	DECADE COUNTER
TC5027BP	BINARY COUNTER
TC5029BP	QUAD 2-INPUT NAND +N CHAN OPEN DRAIN
TC5032P	6-DIGIT DECADE COUNTER
TC5036P	17-STAGE HIGH SPEED FREQUENCY DIVIDER (DYNAMIC)
TC5037P	4-DIGIT DECADE COUNTER
TC5048P	17-STAGE HIGH SPEED FREQUENCY DIVIDER (DYNAMIC)
TC5050P	DUAL 50/64-BIT STATIC SHIFT REGISTER
TC5051P	4 DIGIT DECADE COUNTER WITH/BLANKING COUNTROL
TC5052P	4 DIGIT DECADE COUNTER WITH/CLOCK ENABLE
TC5053P	4 DIGIT UP/DOWN DECADE COUNTER
TC5054P	4 DIGIT UP/DOWN DECADE COUNTER
TC5055P	$3\frac{1}{2}$ DIGIT DVM CIRCUIT
TC5064BP	HEX HIGH VOLTAGE BUFFER WITH INHIBIT/NON INVERTING
TC5065PB	HEX HIGH VOLTAGE BUFFER WITH INHIBIT/INVERTING
TC5066BP	7-HIGH VOLTAGE BUFFER/NON INVERTING
TC5067BP	7-HIGH VOLTAGE BUFFER/INVERTING

TC7400 Series

Product Name	Function
TC7400BP	QUAD 2-INPUT POSITIVE NAND GATE
TC7404UBP	HEX INVERTER
TC7476BP	DUAL J-K MASTER-SLAVE FLIP FLOP

〔1〕 EXPLANATION

[1] EXPLANATION

1. C^2MOS IC Family

1.1 C^2MOS

C^2MOS (C Square MOS) is the abbreviation of Clocked CMOS which was released as a circuit application of CMOS by TOSHIBA in 1973 and is extremely efficient switching method used in CMOS circuit.

Therefore, the trade mark of C^2MOS is commonly used for our CMOS ICs including ones which do not have the clocked gates. C^2MOS ICs are named as follows.

TC $\boxed{xxxx}$ P or TC $\boxed{xxxx}$ BP

The first two alphabetic characters are the abbreviation of TOSHIBA CMOS and the following four or five digits of numeric characters are for classifying the functions of products.

The last character, P indicates that the type of sealing is plastic package and the products having "B" (including the products having "UB") between the product number and "P" have the unified operating voltage range of 3 to 18 volts satisfying the standard specifications of JEDEC, namely so called "B Series" products.

C^2MOS IC family can be classified into the following four series based on the compatibility.

(1) TC4000B Series (Pin to pin compatible with RCA CD4000B Series.)
(2) TC4500B Series (Pin to pin compatibel with MOT MC14500B Series.)
(3) TC5000B Series/TC5000 Series (TOSHIBA's original products)
(4) TC7400B Series (Same functions as TTL SN7400 Series.)

As descrived above, although there are products of "B Sereis" and non "B Series" in TC5000 Series, all other series are compatible products having the common operating voltage range of 3 to 18 volts.

The basic development concept of C^2MOS IC family is as follows. For the products of SSI/MSI classes, we develop TC4000B/TC4500B Series because compatibility should be emphasized. On the other hand for the LSI classes we develop original products in TC5000 Series because there are few standard products available from other companies.

A reason of having non "B Series" products in TC5000 Series is that it has big cost merit for LSI to design with the operating voltage range of around 5 volts instead of standard 18 volts.

1.2 TOSHIBA B Series C^2MOS IC

As in the past time there had not been any specification system established by the official organization for standard logic CMOS ICs, each IC Maker had guaranteed based on its own specification system. In July 1976 the standard specifications for standard logic CMOS products called "B" Series were publicized by EIA/JEDEC, and several companies in the United States released already "B" Series products in 1977.

TOSHIBA "B" Series C^2MOS satisfy all the standard specifications of JEDEC and have the following features.

1) Wide operating voltage range of 3 to 18 volts.
2) All the outputs have buffers.
3) Directly drive two LTTL (low power TTL) inputs and one LSTTL (low power Schottky TTL) input.
4) Electrical parameters are guaranteed at three supply voltages of 5, 10 and 15 volts.
5) Classified to "B" and "UB" based on the circuit configuration and the noise immunity.
6) The noise immunity of "B" Type is as follows.

1V	(Min.)	@ V_{DD} = 5V
2V	(Min.)	@ V_{DD} = 10V
2.5V	(Min.)	@ V_{DD} = 15V

2. Operational Principle and Features of CMOS

2.1 Basic circuit and structure of CMOS

Inverter circuit is taken as an example of CMOS basic circuit. CMOS inverter, as shown in Fig. 1-1, consists of the common input terminal shared by P-channel enhancement (normally off) type MOS FET and N-channel enhancement type MOS FET and the common output terminal shared by each drain.

As shown in the same figure, CMOS inverter uses P-channel and N-channel MOS FETs complementarily.

Usually, the source of P-channel MOS FET is connected to V_{DD} (+supply) and the source of N-channel MOS FET is connected to V_{SS} (usually GND).

Fig. 1-2 illustrates the cross section using the basic process. N-type silicon is used as substrate for CMOS basic process.

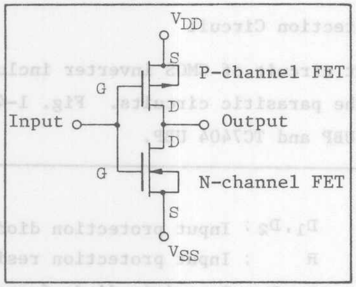


Fig. 1-1. Circuit Diagram of CMOS Inverter

For normal P-channel MOS FETs, P-type impure material is selectively diffused in the domain of N-type substrate to form the source and the drain. For CMOS, however, since N-channel MOS FET is also required to be formed in same substrate, after forming P-type island domain (P-well) in N-type substrate by means of ion implanation, N-channel MOS FET is formed in this P-well. And P-channel MOS FET is formed in the substrate outside of this island domain.

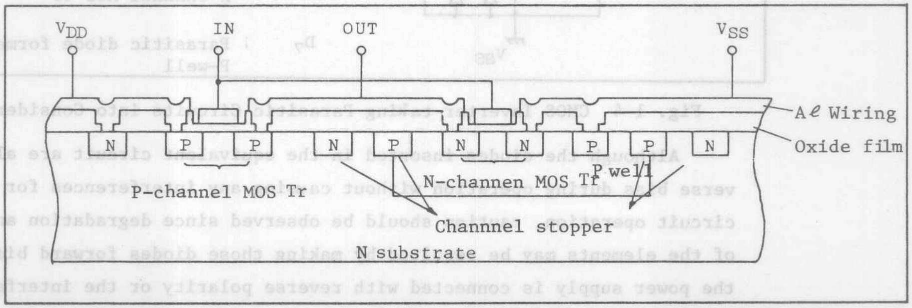


Fig. 1-2 Structural Cross Section of Aℓ Gate CMOS

N-type substrate and P-well are separated (reverse biased) by V_{DD} and V_{SS}. Therefore, P-channel and N-channel FETs operate independently each other with no mutual interferences.

Fig. 1-2 is the basic cross section of CMOS inverter. The static protection circuit is inserted in the input gate as shown in Fig. 1-3 for the actual products.

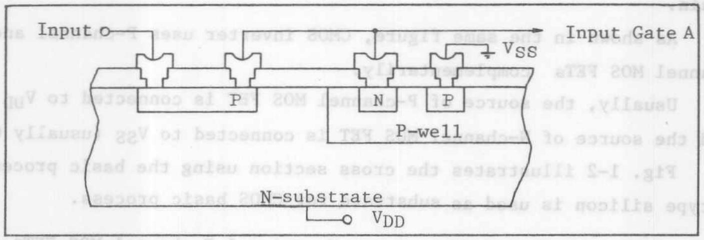
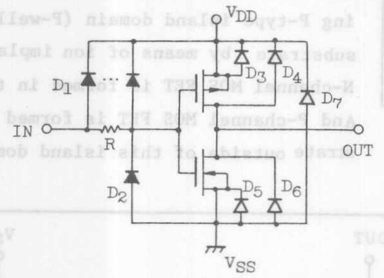


Fig. 1-3 CMOS Input Protection Circuit

Fig. 1-4 shows the equivalent circuit of CMOS inverter including the input protection circuit and the parasitic circuits. Fig. 1-4 actually represents the circuits of TC4069 UBP and TC7404 UBP.



D_1, D_2 ; Input protection diode
R ; Input protection resistor
D_3, D_4 ; Parasitic diode formed by P-channel MOS Tr
D_5, D_6 ; Parasitic diode formed by N-channel MOS Tr
D_7 ; Parasitic diode formed by P-well

Fig. 1-4 CMOS Inverter taking Parasitic Circuits into Consideration

Although the diodes inserted in the equivalent circuit are all reverse bias during operation without causing any interferences for normal circuit operation, caution should be observed since degradation and damage of the elements may be resulted by making those diodes forward biased when the power supply is connected with reverse polarity or the interface is driven roughly.

2.2 Basic characteristics of CMOS

CMOS is a classification based on the circuit configuration and the characteristics of each MOS FET actually used are equal to common enhancement type FETs.

Therefore, in the case of CMOS also, the characteristics of P-channel and N-channel MOS FETs can be basically approximated by Shockley's equation.

$$I_{DS} = K\,[2V_{DS}(V_{GS} - V_T) - V_{DS}{}^2],\quad V_{DS} < V_{GS} - V_T \quad \ldots\ldots (1.1)$$

$$I_{DS} = K\,(V_{GS} - V_T)^2,\quad V_{DS} \geqq V_{GS} - V_T \quad \ldots\ldots (1.2)$$

$$I_{DS} = 0,\quad V_{GS} \leqq V_T \quad \ldots\ldots (1.3)$$

Where the constant K is

$$K = \frac{W}{2L} \cdot \frac{Eox}{tox} \cdot \mu$$

- L ; Channel length
- W ; Channel width
- Eox ; Dielectric constant of gate oxide film
- tox ; Thickness of gate oxide film
- μ ; Mobility of electron or positive hole
- V_{DS} ; Potential difference between drain and source
- V_{GS} ; Potential difference between gate and source
- V_T ; Threshold voltage

Using the above approximation equations (1.1) ~ (1.3), the basic characteristics are explained below taking inverter as an example.

(1) Transfer characteristic of inverter

The input voltage, the output voltage and the power supply voltages are assumed to be V_{IN}, V_{OUT} and $+V_O$ volts respectively. The threshold voltages are assumed to be V_{TP} for P-channel FET and V_{TN} for N-channel FET respectively.

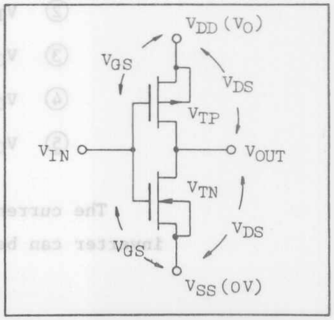


Fig. 1-5 Relationships of Various Bias

Here, V_{TP} is considered to have negative value and V_{TN} to have positive value. As it is clear from Fig. 1-5, V_{DS} and V_{GS} which appeared in equations (1.1) ~ (1.3) are

$$V_{DS} = V_{OUT} \text{ , } V_{GS} = V_{IN}$$

for N-channel FET.

So, equations (1.1) ~ (1.3) can be rewritten as shown below

$$I_{DSN} = K_N \left[2V_{OUT}(V_{IN}-V_{TN})-V_{OUT}^2\right], \quad V_{OUT} < V_{IN} - V_{TN} \; \ldots \; (1.4)$$

$$I_{DSN} = K_N (V_{IN} - V_{TN})^2 \quad , \quad V_{OUT} \geqq V_{IN} - V_{TN} \; \ldots \; (1.5)$$

$$I_{DSN} = 0 \quad , \quad V_{IN} \leqq V_{TN} \; \ldots \; (1.6)$$

On the other hand, since

$$V_{DS} = V_O - V_{OUT} \text{ AND } V_{GS} = V_O - V_{IN}$$

for P-channel, equations (1.1) ~ (1.3) can be rewritten as follows.

$$I_{DSP} = K_P\left[2(V_O-V_{OUT})(V_O-V_{IN}-|V_{TP}|)-(V_O-V_{OUT})^2\right],$$

$$V_{OUT} > V_{IN} + |V_{TP}| \; \ldots\ldots \; (1.7)$$

$$I_{DSP} = K_P(V_O-V_{IN}-|V_{TP}|)^2, V_{OUT} \leqq V_{IN} + |V_{TP}| \; \ldots\ldots \; (1.8)$$

$$I_{DSP} = 0 \quad , V_{IN} + |V_{TP}| \geqq V_O \; \ldots\ldots \; (1.9)$$

When the input voltage of inverter varies from 0 volts to V_O volts, the operating range of each MOS FET can be classified into the following five regions.

① $0_V \leqq V_{IN} \leqq V_{TN}$

② $V_{TN} < V_{IN} < V_{OUT} - |V_{TP}|$

③ $V_{OUT} - |V_{TP}| \leqq V_{IN} \leqq V_{OUT} + V_{TN}$

④ $V_{OUT} + V_{TN} < V_{IN} < V_O - |V_{TP}|$

⑤ $V_O - |V_{TP}| \leqq V_{IN} \leqq V_O$

The currents in the above five regions for each FET forming the inverter can be represented by equations (1.4) ~ (1.9) respectively.

When the input/output transfer characteristic is to be obtained, since the current carried by P-channel, I_{DSP} is equal to the current carried by N-channel, I_{DSN}, the transfer characteristic in each region is obtained by making $I_{DSN} = I_{DSP}$.

Especially, by making $I_{DSN} = I_{DSP}$ in the equations (1.5) and (1.8) of current in the region of ②, the following equation is obtained.

$$V_{IN} = \frac{V_{TN}\left(\sqrt{\frac{K_N}{K_P}}\right) + V_O - |V_{TP}|}{1 + \left(\sqrt{\frac{K_N}{K_P}}\right)}$$

Fig. 1-6 shows the comparison between the theoretical values obtained by those equations and the measuring values.

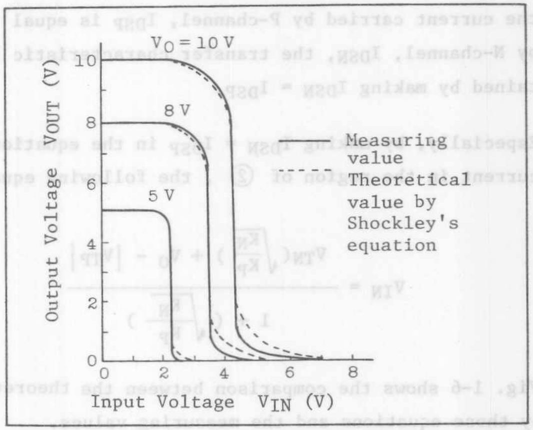


Fig. 1-6 Input/Output Transfer Characteristic

(2) Step response of inverter

When step input which varies from 0 volts to $+V_O$ volts is applied to the inverter input, P-channel FET is turned off and N-channel FET is turned on. As a result, electrical charge stored in the load capacitor C_{OUT} is discharged through N-channel FET and the output voltage V_{OUT} varies from $+V_O$ volts to 0 volts as the discharge proceeds.

a) When $V_{OUT} \geqq V_O - V_{TN}$

The equation for current is given by (1.5) and since C_{OUT} is discharged by this current,

$$- I_{DSN} = C_{OUT} \frac{d\,V_{OUT}}{dt}, \quad V_{OUT}=V_O \text{ at } t = 0$$

When this is integrated,

$$\int_0^t dt = -\int_{V_O}^{V_{OUT}} \frac{C_{OUT}}{K_N(V_O-V_{TN})^2} \cdot dV_{OUT}$$

Namely,

$$t = \frac{C_{OUT}}{K_N(V_O - V_{TN})^2} (V_O - V_{OUT}) \quad \text{.......... (1.10)}$$

If t_0 is defined at $V_{OUT} = V_0 - V_{TN}$,

$$t_0 = \frac{C_{OUT} \cdot V_{TN}}{K_N(V_0 - V_{TN})^2}$$

b) When $V_{OUT} \leqq V_0 - V_{TN}$

If integrated similarly as a) using equation (1.4),

$$\int_0^t dt = \frac{-C_{OUT}}{2K_N(V_0-V_{TN})} \times \int_{V_0-V_{TN}}^{V_{OUT}} \left\{ \frac{1}{V_{OUT}} + \frac{1}{2(V_0-V_{OUT})-V_{OUT}} \right\} dV_{OUT}$$

Then,

$$t = \frac{C_{OUT}\, V_{TN}}{K_N(V_0-V_{TN})} + \frac{C_{OUT}}{2K_N(V_0-V_{TN})} \ell n \left[\frac{2(V_0-V_{TN})-V_{OUT}}{V_{OUT}}\right] \quad ..... (1.11)$$

As the fall time t_f is the time required for the output voltage to vary from 90% to 10%, if t_1 is assumed to be the time for the output voltage to reach 90% of V_0 and t_2 is assumed to be the time to reach 10% of V_0, t_1 and t_2 are given from equations (1.10) and (1.11) as follows.

$$t_1 = \frac{C_{OUT}}{K_N(V_0-V_{TN})^2} \times 0.1V_0$$

$$t_2 = \frac{C_{OUT}\, V_{TN}}{K_N(V_0-V_{TN})^2} + \frac{C_{OUT}}{2K_N(V_0-V_{TN})} \ell n \left[\frac{2(V_0-V_{TN})-0.1V_0}{0.1V_0}\right]$$

Therefore,

$$t_f = t_2 - t_1 = \left\{ \frac{V_{TN}-0.1V_0}{V_0-V_{TN}} + 1/2\ \ell n \left[20\left(1-\frac{V_{TN}}{V_0}\right)-1\right] \right\} \times \tau_N \quad ...(1.12)$$

$$\text{where} \left\{ \begin{aligned} \tau_N &= \frac{C_{OUT}}{K_N(V_0-V_{TN})} \\ K_N &= 1/2 \cdot \frac{\varepsilon_{OX}\, \mu_N}{t_{OX}} \cdot \frac{W_N}{L_N} \end{aligned} \right\}$$

The rise time t_r can be obtained similarly and the result will be the same as equation (1.12) except that N is replaced by P.

2.3 Features of CMOS

Table 1-1 compares the characteristics of logic families including CMOS. From this table it is clear that although the speed is slower than others, the power consumption in quiescent state and the noise immunity are far superior to others.

And since CMOS has wider operating supply voltage range, the supply voltage can be flexibly set according to the applications and where to be used.

Table 1-1 Comparison of Various Logic Families

Parameter (typical values)	Standard TTL	Low power TTL	Low power Schottky TTL	DTL	CMOS (5V)	CMOS (10V)
Propagation Delay Time (ns)	10	33	5 ~ 10	30	70	35
F/F Toggle Frequency (MHz)	35	3	40 ~ 80	5	3	6
Quiescent Power Consumption (mW)	10	1	8.5	2	5×10^{-6}	2×10^{-5}
Noise Immunity (V)	1	1	0.8	1	2	4
Fanout	10	10	20	8	50	50

(1) Propagation delay and F/F toggle frequency

As shown by equation (1.12) in 2.2, the propagation delay of CMOS is proportional to C_{OUT} (load capacitance) and inversely proportional to the constant K_N which is determined by design and process.

Therefore, in order to make the propagation delay shorter, it is necessary to make C_{OUT} smaller and W/L in design considerations. However, since the internal diffusion capacitance in CMOS is included in C_{OUT}, the internal capacitance increases proportionally to W/L and actually the propagation delay tends to have a limitation.

In the standard C^2MOS ICs the propagation delay time is determined by balancing other electrical parameters since there are other limitations such as the output current and the breakdown voltage causing to have larger value than other logic elements as shown in Table 1-1.

However, the products for specific applications and CMOS ICs having the capabilities of high speed operations for the high speed frequency divider are currently being developed, and the speed of around 10ns delay per internal stage of CMOS at 5 volts has been obtained providing the expectation that the product range of such CMOS will be expanded for the systems requiring the high frequency operations in the future.

(2) Quiescent (Static) power consumption and operating power consumption

In the standard CMOS, when the input holds "L" (V_{SS}) level or "H" (V_{DD}) level, N-channel FET or P-channel FET is kept turned off. So, the current from V_{DD} to V_{SS} is limited to the reverse direction saturation current of PN junction and the surface leakage current caused mainly by contamination on the chip surface; consequently, the value is only 1nA～2nA at the normal temperature for gate ICs.

In the case of other logic circuits except CMOS, when the output driving transistor is turned on, direct current flows down from V_{CC} to GND through the load causing the power consumption in the quiescent state to be approximately equal to the operating power consumption.

The operating power consumption of CMOS can be considered to be only the switching power loss which is generated to charge/discharge the load capacitance while inverting the logical levels, so that the operating power consumption is proportional to the switching frequency.

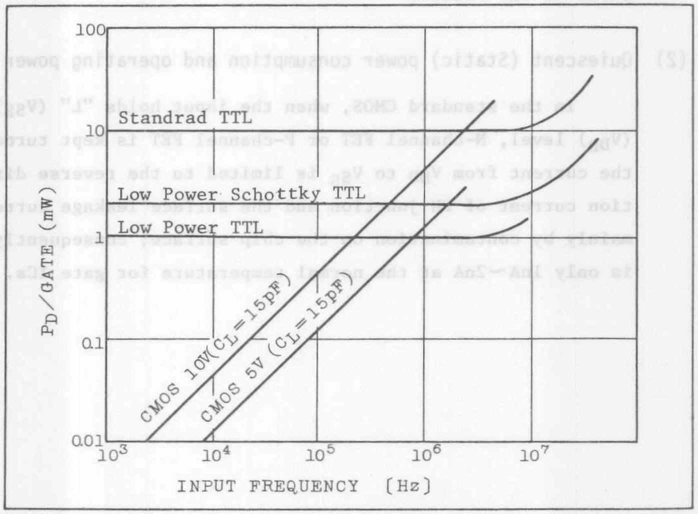


Fig. 1-7 Operating frequency VS Power Consumption of CMOS/TTL

Fig. 1-7 shows the relationship between the operating frequency and the power consumption of TTL and CMOS. As shown in the figure, the advantages of CMOS will be fully utilized at the operating frequency lower than 10^6Hz.

(3) Noise immunity

For CMOS circuits as shown in Fig. 1-6, since the device threshold voltage is ideally set to the mid-point of supply voltage, the maximum noise immunity can be obtained among the various logic devices. It can be seen from the same figure that the standard value of noise immunity for CMOS is 2 volts (at V_{DD} = 5V) or 4 volts (at V_{DD} = 10V), which are considerably larger than the value of 1 volt for TTL.

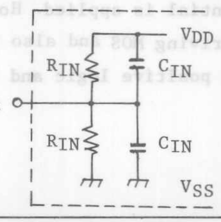
The device threshold voltage of CMOS, however, is determined by ON-resistance ratio of P-channel and N-channel MOS FETs and directly affected by the variations of those values. Therefore, the noise immunity guaranteed in the catalog of "B Series" products is 1 volt (at V_{DD} = 5V) or 2 volts (at V_{DD} = 10V), and attention should be paid to this point.

(4) Fanout

Since the protection diodes are reversely biased as long as rating voltages ($V_{SS} \sim V_{DD}$) are applied, CMOS input has extremely high DC impedance ($R_{IN} \fallingdotseq 10^{11}\Omega$).

Furthermore, since the gate of MOS FET equivalently funcitons as one of electrodes of parallel plate capacitor, AC characteristic indicates the capacitive value of approximately 5pF.

This situation can be illustrated as shown in Fig.1-8. These resistive component and capacitive component are inserted in parallel to V_{DD} side and V_{SS} side.



R_{IN} ; $10^{10} \sim 10^{12}$ Ω

C_{IN} ; 3 ~ 5 pF

Fig. 1-8 Equivalent Circuit of CMOS Input

Therefore, in order to drive CMOS input, only very little current is required electrically to supply or to drain. This fact means that the output impedance of normal CMOS is around 200 ~ 1K Ω which makes it possible to drive the almost unlimited number of CMOS in DC operation.

However, as the number of fanout increases (n, for example), all of input capacitance C_{IN} are connected in parallel, increasing the load capacitance of output. So, the load capacitance viewed from the driving side is,

$$C_L = n \cdot C_{IN} + C_S \quad \text{(1.13)}$$

C_S : Stray capacitance generated by wiring, etc.

and this C_L causes the propagation delay time to increase.

Considering these situations, the practical number of fanout for C^2MOS has been determined to be 50. The fact that 50 fanouts can be actually provided eliminates almost all restrictions in the wiring arrangements of wired logic circuits.

3. Basic Circuit of CMOS

3.1 Positive logic and negative logic

The difference between positive logic and negative logic is only conceptual difference and it can not be said that the positive logic should be used for CMOS.

The negative logic is easier to consider about P-channel MOS device due to the fact that negative supply voltages are used and that FET is turned on when negative potential is applied. However in CMOS both P-channel and N-channel are the driving MOS and also the load MOS, so the conditions are same for the positive logic and the negative logic.

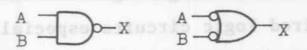
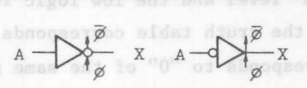
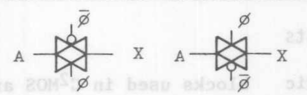
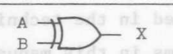
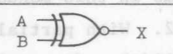
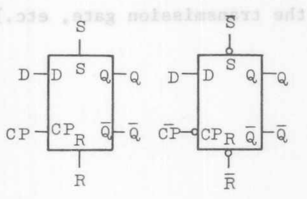
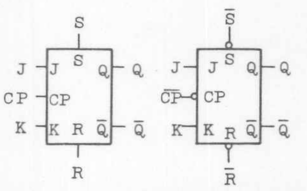
It has been decided that C^2MOS family is described in the positive logic in the catalog because of the facts that the positive logic is easier to handle for the design engineers who are familiar with the design works of wired logic circuits especially with TTL and that recently N-channel LSI become more and more popular and the positive logic is more convenient for the interfaces.

In order to avoid any confusion on the positive logic and the negative logic of the truth table, the potentially high logic level si described to be "H" level and the low logic level to be "L" level. Therefore, "H" in the truth table corresponds to "1" of the positive logic and "L" corresponds to "0" of the same positive logic.

3.2 Basic logic circuits

The basic logic blocks used in C^2MOS are shown in Table 1-2. The logic diagrams illustrated in the technical bulletin of each product and the logic diagrams in this manual are configured by the basic blocks shown in Table 1-2. With partial exceptions, these logic diagrams are based on MIL-STD806(C). (Special symbols are used for the clocked inverter, the transmission gate, etc.)

Table 1-2 Basic Logical Circuits

<table>
<tr><th>Circuit Function</th><th>Logical Symbol</th><th>Logical Equation or Truth Table</th></tr>
<tr><td>Inverter</td><td></td><td>$X = \bar{A}$</td></tr>
<tr><td>NAND Gate</td><td></td><td>$X = \overline{A \cdot B} = \bar{A} + \bar{B}$</td></tr>
<tr><td>NOR Gate</td><td></td><td>$X = \overline{A+B} = \bar{A} \cdot \bar{B}$</td></tr>
<tr><td>AND Gate</td><td></td><td>$X = A \cdot B = \overline{\bar{A}+\bar{B}}$</td></tr>
<tr><td>OR Gate</td><td></td><td>$X = A+B = \overline{\bar{A} \cdot \bar{B}}$</td></tr>
<tr><td>Clocked Inverter</td><td></td><td><table><tr><td>Ø</td><td>A</td><td>X</td></tr><tr><td>H</td><td>H</td><td>L</td></tr><tr><td>H</td><td>L</td><td>H</td></tr><tr><td>L</td><td>※</td><td>HZ</td></tr></table>※ ; Don't Care
HZ;High Impedance</td></tr>
<tr><td>Transmission Gate</td><td></td><td><table><tr><td>Ø</td><td>A</td><td>X</td></tr><tr><td>H</td><td>H</td><td>H</td></tr><tr><td>H</td><td>L</td><td>L</td></tr><tr><td>L</td><td>※</td><td>HZ</td></tr></table>※ ; Don't Care
HZ;High Impedance</td></tr>
<tr><td>EXCLUSIVE - OR Gate</td><td></td><td>$X = (A+B) \cdot (\bar{A}+\bar{B})$</td></tr>
<tr><td>EXCLUSIVE - NOR Gate</td><td></td><td>$X = (A \cdot B)+(\bar{A} \cdot \bar{B})$</td></tr>
<tr><td>D - Type Flip - Flop</td><td></td><td><table><tr><td>S</td><td>R</td><td>D</td><td>CP</td><td>Q</td></tr><tr><td>H</td><td>L</td><td>※</td><td>※</td><td>H</td></tr><tr><td>L</td><td>H</td><td>※</td><td>※</td><td>L</td></tr><tr><td>L</td><td>L</td><td>H</td><td>↑</td><td>H</td></tr><tr><td>L</td><td>L</td><td>L</td><td>↑</td><td>L</td></tr><tr><td>L</td><td>L</td><td>※</td><td>↓</td><td>Q_n △</td></tr></table>※ ; Don't Care
△ ; No Change</td></tr>
<tr><td>J/K Type Flip - Flop</td><td></td><td><table><tr><td>S</td><td>R</td><td>J</td><td>K</td><td>CP</td><td>Q</td></tr><tr><td>H</td><td>L</td><td>※</td><td>※</td><td>※</td><td>H</td></tr><tr><td>L</td><td>H</td><td>※</td><td>※</td><td>※</td><td>L</td></tr><tr><td>L</td><td>L</td><td>L</td><td>L</td><td>↑</td><td>Q_n</td></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>↑</td><td>L</td></tr><tr><td>L</td><td>L</td><td>H</td><td>L</td><td>↑</td><td>H</td></tr><tr><td>L</td><td>L</td><td>H</td><td>H</td><td>↑</td><td>Q_{n+1} ▽</td></tr><tr><td>L</td><td>L</td><td>※</td><td>※</td><td>↓</td><td>Q_n △</td></tr></table>※ ; Don't Care
△ ; No Change
▽ ; Toggle</td></tr>
</table>

3.3 Configuration of basic circuit

(1) NAND/NOR

CMOS NAND gate, as illustrated in Fig. 1-9 i), is formed by connecting P-channel FETs in parallel between V_{DD} and the output and by connecting N-channel FETs in series between V_{SS} and the output.

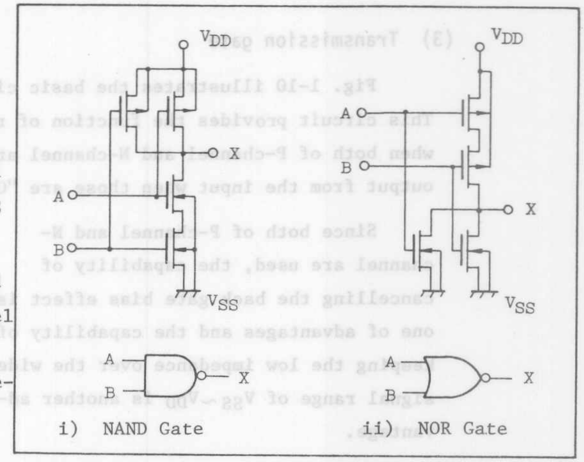


Fig. 1-9 NAND/NOR Gate

When both inputs A and B are "H", both of N-channel FETs in series are turned on, causing the impedance between X and V_{SS} to be low. at this time, both of P-channel FETs are turned off cutting off X from V_{DD}. Therefore, the output becomes nearly equal to V_{SS} generating "L" level. In the case of other input modes, at last one of P-channel FETs is turned on and one N-channel FETs are turned off causing the output to be "H" level.

NOR gate of ii) in Fig. 1-9 is fabricated in the reversed way of NAND gate i) to generate "H" output only when both of inputs A and B are "L".

The gates with 3 inputs or more can be realized with the same configuration simply by increasing the number of stages of P-channel or N-channel FETs in series or in parallel. In the case of C^2MOS up to around four inputs the device can be configured with one stage, but the gates with more inputs are realized by combining the basic circuits.

(2) AND/OR

Since the output is always inverted by one stage of CMOS gate, AND gate and OR gate are realized by adding an inverter to the output of NAND/OR of (1).

Therefore, it is important for CMOS MSI/LSI to effectively combine NAND/NOR rather than to fabricate the gates with AND/OR, in order to reduce the number of elements.

(3) Transmission gate

Fig. 1-10 illustrates the basic circuit of transmission gate. This circuit provides the function of reed switch which transmits the data when both of P-channel and N-channel are "ON" (c="H") and separates the output from the input when those are "OFF" (C="L").

Since both of P-channel and N-channel are used, the capability of cancelling the back gate bias effect is one of advantages and the capability of keeping the low impedance over the wide signal range of $V_{SS} \sim V_{DD}$ is another advantage.

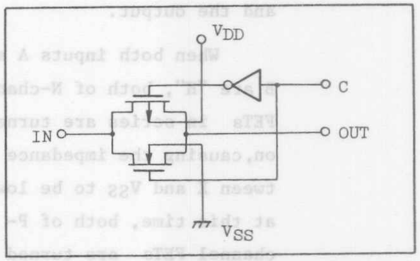


Fig. 1-10 Transmission Gate

The applications would be as follows.

i) Switching functions of sequencial circuits, such as shift registers, counters, etc.

ii) Analog switches iii) 3-stage gates*

*3-state gates: 3-state is named for the capability of providing three states of output which are normal "H", normal "L" and high impedance condition not being connected to V_{DD} or V_{SS}, namely not "H" nor "L". This characteristic can be applied for the intervace with bus line of process control systems and multiplexers.

(4) Clocked gate

When a delay circuit or a switching circuit is required, the transmission gate is usually used. However, this circuit has a disadvantage that the pattern becomes more complicated with increased area when the circuit is to be integrated in LSI. The one which overcomes this disadvantage keeping the characteristics of conventional transmission gate is the clocked gate (clocked inverter) shown in Fig. 1-11.

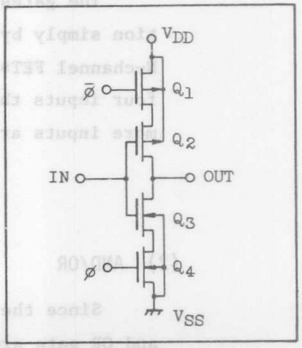


Fig. 1-11 Clocked Gate

Q_2 and Q_3 are normal configuration of inverter, however by serially inserting Q_1 and Q_4 in the circuit, the function of normal inverter can be obtained when Q_1 and Q_4 are "ON" (ϕ="H") and the output has high impedance when Q_1 and Q_4 are "OFF" (ϕ="L").

Although this circuit does not have the functions of analog switch, all the other functions of transmission gate are provided.

If the concept of this clocked inverter is expanded, clocked NAND and clocked NOR can be realized.

(5) Exclusive OR/Exclusive NOR

Exclusive OR is also called coincidence circuit which gives the output of "L" when all the inputs are at "H" or "L" level and gives the output of "H" when at least one of inputs differs from others.

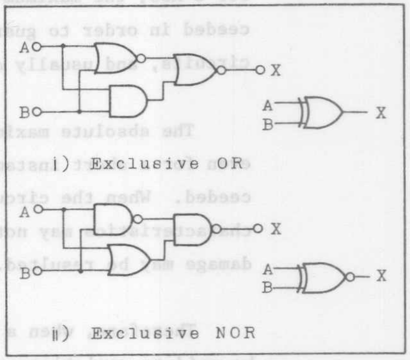


Fig. 1-12 Exclusive OR/NOR

Exclusive NOR is the one with the inverted output of the above exclusive OR and gives the output of "H" when all the inputs coincide at "H" or "L" level.

Fig. 1-12 illustrates the configurations of these circuits.

(6) D-type flip-flop/J-K type flip-flop

These will be explained in the chapter of Flip-Flops.

4. Maximum Ratings and Recommended Operating Conditions

4.1 Maximum ratings

The maximum ratings are specified for each C^2MOS product. Not only for C^2MOS, the maximum ratings are the values which should not be exceeded in order to guarantee the life and the reliability of integrated circuits, and usually considered to be the absolute maximum ratings.

The absolute maximum ratings are the values which may not be exceeded even for a short instance and none of any rating values may not be exceeded. When the circuits are used exceeding the maximum ratings, their characteristics may not be recovered and in extreme cases permanent damage may be resulted.

Therefore, when a circuit is designed, extreme attention should be paid to variations of supply voltages, characteristics of connected components, surges of input/output signal lines, environment temperature, etc. Table 1-3 lists the common maximum ratings of B series C^2MOS.

When the maximum ratings of each product differ from the common ratings, the former takes precedence.

Table 1-3 Common Maximum Ratings of B Series C^2MOS

CHARACTERISTIC	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300	mW
Storage Temp.	Tstg	$-65 \sim 150$	°C
Lead Temp./Time	Tsol	260°C·10 sec	

(1) Supply voltage

This is supply voltage applied between V_{DD} terminal and V_{SS} terminal. Usually biased to satisfy $V_{DD} > V_{SS}$ and the reverse bias due to the undershoot of power supply, etc. should be limited to -0.5 volts.

If higher voltage than this value is given in the condition of $V_{SS} > V_{DD}$, the parasitic diode D_7 shown in Fig. 1-4 is forward biased causing excessive current to flow from V_{SS} to V_{DD} and in extreme cases, the element may be damaged.

The upper limit of 20 volts is established based on the breakdown voltages of parasitic diodes and transistors of various circuits, and the value should never be exceeded. If voltage applied exceeding the rating, CMOS device may reach to the secondary breadown region of latch-up, etc. from the primary breakdown region.

Since V_{SS} is set to GND (0 volts) in most cases, the voltage of V_{DD} terminal should be considered to be in the range of -0.5 ~ 20 volts.

(2) Input voltage and output voltage

The electrostatic protection diodes are inserted in the input as shown in Fig.1-3 and Fig.1-4. These diodes are not installed to absorb the current fed from outside but installed to protect the input oxide film from the destruction caused by electrostatic charge.Therefore,the input voltage is limited to the range that the input protection diodes are not forward biased. The lower limit is V_{SS} -0.5 volts and the upper limit is V_{DD} +0.5 volts.

The output terminal is used usually to drive CMOS and other electronic components and although any voltage is not applied from outside,situations where the voltage transiently varies due to the external surge or driving of a capacitive load or an inductive load may possibly exist. If the output voltage exceeds the range of $V_{SS} \sim V_{DD}$ in this case, D_4 and D_6 of Fig. 1-4 are forward biased causing excessive current to flow from the output to V_{DD} or from V_{SS} to the output.

As this current possibly causes primary damage of opening the output line and secondary damage of latch-up, the output voltage is similarly as the input specified as a rating to be in the range of V_{SS} - 0.5 volts ~ V_{DD} + 0.5 volts to prevent the parasitic diode to be forward biased.

(3) Input current

This item may seem to be contradictory with the rating of input voltage (2), but this indicates the critical value at which the input protection diodes and other elements will not be destroyed or degraded when voltages exceeding the ratings are applied due to surges caused by interfaces. Therefore it is not recommended to design circuits which flow DC current through the input protection diodes. Even when it can not be avoided to apply voltage causing current to flow to the input, the current should be limited to 1 mA or less.

(4) Power dissipation

As far as CMOS is used in a normal manner, the power dissipation is extremely small not causing any problems concerning the allowable loss. However, when LED is driven or big current is driven by the buffer, power is consumed in CMOS. For C^2MOS, the power dissipation is specified to be 300 mW per package.

Since the power consumption in the internal circuit can be neglected for C^2MOS in most cases comparing with that of the output stage, the power consumption can be calculated only considering the output stage.

(5) Storage temperature

This indicates the ambient temperature at which degradation of characteristics or reliability is not resulted even if the products are exposed in the environment for long time without applying the supply voltage. In the case of C^2MOS, the storage temperature range of -65°C ~ 150°C is specified as the rating.

(6) Lead temperature and time

These are conditions which should be limited when soldered after mounting C^2MOS on the printed circuit board. Regardless whether a solder pot is used or a soldering iron is used, the lead temperature should be limited up to 260°C and soldering should be completed within 10 sec. When a solder pot is used, the area which is allowed to dip into solder is up to the stopper of IC lead frame.

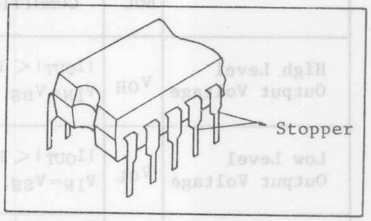


Fig.1-13 External appearance

4.2 Recommended operating conditions

These are the ranges where the operations of C^2MOS IC are guaranteed and when the ranges are exceeded the operations are not guaranteed even if such ranges are inside of the maximum ratings. Therefore, it is important to use the products inside of these ranges.

Table 1-4 Common Recommended Operating Conditions of C^2MOS (V_{SS}=0V)

Item	Symbol	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	3	-	18	V
Input Voltage	V_{IN}	0	-	V_{DD}	V
Operating Temp.	Topr	-40	-	85	°C

Table 1-4 lists the common recommended operating conditions of B series C^2MOS. When the recommended operating conditions of each product differ from the common recommended operating conditions, the former takes precedence.

(1) Power supply voltage

Wide range of operating power supply voltage, 3 volts ~18 volts from V_{SS} is guaranteed for B series C^2MOS. The lower limit of 3 volts is determined by V_T of P-channel and N-channel FETs and when the voltage becomes lower than this value, V_{GS} gets so small that the normal operations of CMOS can not be expected. The upper limit of 18 volts is determined by the breakdown voltage.

(2) Operating temperature

This is the temperature range where the normal operations and characteristics of IC are guaranteed. The operations of B series C^2MOS are guaranteed in the wide range of -40°C ~ 80°C.

Table 1-5 Electrical Characteristics of TC4001BP (V_{SS}=0V)

ITEM		SYM-BOL	TEST CONDITIONS	V_{DD} (V)	-40℃		25℃			85℃		
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\lvert I_{OUT}\rvert < 1\mu A$ $V_{IN}=V_{SS}$	5	4.95	—	4.95	5.00	—	4.95	—	V
				10	9.95	—	9.95	10.00	—	9.95	—	
				15	14.95	—	14.95	15.00	—	14.95	—	
Low Level Output Voltage		V_{OL}	$\lvert I_{OUT}\rvert < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	
				10	—	0.05	—	0.00	0.05	—	0.05	
				15	—	0.05	—	0.00	0.05	—	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V	5	-0.2	—	-0.16	-0.5	—	-0.12	—	mA
			V_{OH}=9.5V	10	-0.5	—	-0.4	-1.2	—	-0.3	—	
			V_{OH}=13.5V $V_{IN}=V_{SS}$	15	-1.4	—	-1.2	-6.0	—	-1.0	—	
Low Level Output Current		I_{OL}	V_{OL}=0.4V	5	0.52	—	0.44	1.5	—	0.36	—	
			V_{OL}=0.5V	10	1.3	—	1.1	3.5	—	0.9	—	
			V_{OL}=1.5V $V_{IN}=V_{SS}, V_{DD}$	15	3.6	—	3.0	15	—	2.4	—	
High Level Input Voltage		V_{IH}	V_{OUT}=0.5V	5	3.5	—	3.5	2.75	—	3.5	—	V
			V_{OUT}=1.0V	10	7.0	—	7.0	5.5	—	7.0	—	
			V_{OUT}=1.5V $\lvert I_{OUT}\rvert < 1\mu A$	15	11.0	—	11.0	8.25	—	11.0	—	
Low Level Input Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	—	1.5	—	2.25	1.5	—	1.5	
			V_{OUT}=1.0V, 9.0V	10	—	3.0	—	4.5	3.0	—	3.0	
			V_{OUT}=1.5V, 13.5V $\lvert I_{OUT}\rvert < 1\mu A$	15	—	4.0	—	6.75	4.0	—	4.0	
Input Current	"H"Level	I_{IH}	V_{IH}=18V	18	—	0.3	—	10^{-5}	0.3	—	1.0	μA
	"L"Level	I_{IL}	V_{IL}=0V	18	—	-0.3	—	-10^{-5}	-0.3	—	-1.0	μA
Quiescent Supply Current		I_{DD}	$V_{IN}=V_{SS}, V_{DD}$ ※	5	—	1.0	—	0.001	1.0	—	7.5	μA
				10	—	2.0	—	0.001	2.0	—	15	
				15	—	4.0	—	0.002	4.0	—	30	

5. Electrical Characteristics and Switching Characteristics

5.1 Electrical characteristics

Table 1-5 lists the electrical characteristics of TC4001BP.

Excluding the products with special specifications, the guaranty of electrical characteristics and the specifications are standardized, so that each item of TC4001BP (QUAD 2-INPUT NOR GATE) will be explained here.

(1) High level output voltage/low level output voltage (V_{OH}/V_{OL})

Fig.1-4 illustrates the test circuits of V_{OH}/V_{OL}. Each input terminal is connected to V_{SS} or V_{DD} to get the specified logic level at the output. When the output level can not be determined in the cases of counters, etc. the output logic is determined by applying pulses in advance. Since the load conditions are I_{OH}=-1μA and I_{OL}=1μA, and the measurement is taken in the region where I_{DS} of FET is extremely small,

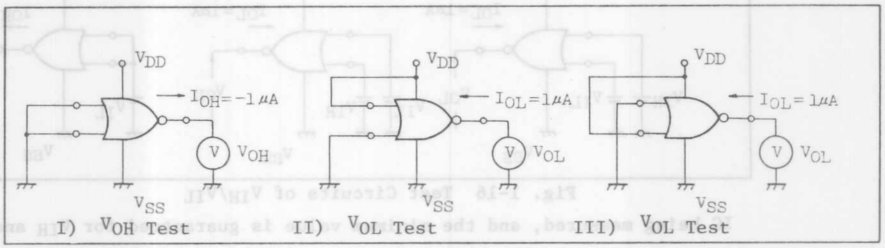


Fig. 1-14 Test Circuits of V_{OH}/V_{OL}

usually $V_{OH} \doteqdot V_{DD}$ and $V_{OL} \doteqdot V_{SS}$. In the cases of interfacing CMOSs each other, the input/output conditions will be approximately equal to the above values. This fact indicated that the switching operation gives the ideal swing from V_{SS} for "L" level of logic signal to V_{DD} for "H" level in CMOS circuits.

(2) High level output current/low level output current (I_{OH}, I_{OL})

Fig.1-15 illustrates the test circuits of I_{OH}/I_{OL}. The input conditions are set in the same manner as for measuring V_{OH}/V_{OL}. In this case, connecting a constant supply voltage to the output to be measured, the current flowing out (I_{OH}) through P-channel FET is measured for high level

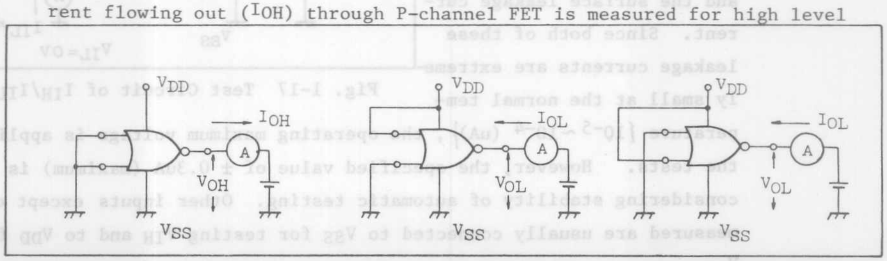


Fig. 1-15 Test Circuits of I_{OH}/I_{OL}

output and the current flowing in through N-channel FET is measured for low level output. These currents are guaranteed at one point in the non-saturation region (also called triode region) of each FET, and the minimum values are guaranteed in the specification table for both I_{OH} and I_{OL}. These can be a guidance to achieve current driving by CMOS output.

(3) High level input voltage/low level input voltage (V_{IH}/V_{IL})

Fig.1-16 illustrates the test circuits of V_{IH}/V_{IL}. V_{IH} and V_{IL} are the voltages which can be recognized as "H" level and "L" level at the input of

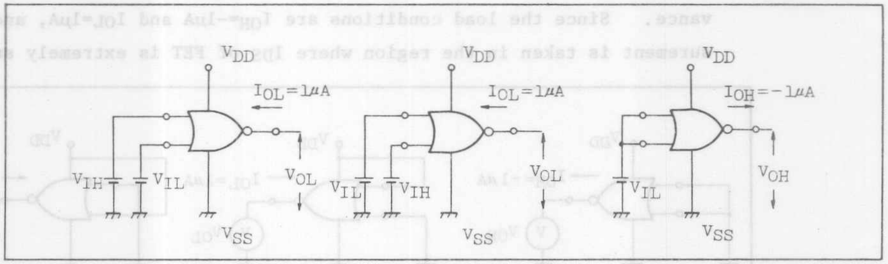


Fig. 1-16 Test Circuits of V_{IH}/V_{IL}

IC being measured, and the minimum value is guaranteed for V_{IH} and the maximum value is guaranteed for V_{IL}. Whether or not IC being measured has correctly recognizes the input level is confirmed by the fact that the output level is at the specified level (higher than V_{OH} or lower than V_{OL} listed in the measurement conditions).

(4) High level input current/low level input current (I_{IH}/I_{IL})

The input current in the range of the ratings of CMOS is considered to be the sum of the reverse current of input protection diode and the surface leakage current. Since both of these leakage currents are extremely small at the normal temperature $\{10^{-5} \sim 10^{-4}\ (uA)\}$, the operating maximum voltage is applied for the tests. However, the specified value of ± 0.3uA (maximum) is guaranteed considering stability of automatic testing. Other inputs except one being measured are usually connected to V_{SS} for testing V_{IH} and to V_{DD} for testing V_{IL}.

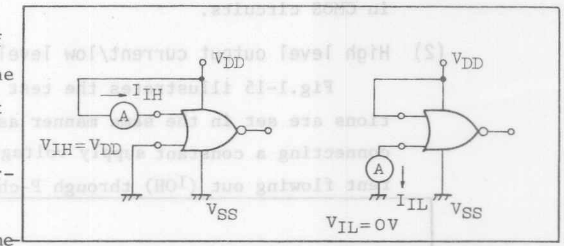


Fig. 1-17 Test Circuit of I_{IH}/I_{IL}

(5) Quiescent supply current (I_{DD})

When CMOS input holds V_{DD} level or V_{SS} level, as described in the paragraph of Features of CMOS, P-channel FET or N-channel FET is always turned off. So, the quiescent supply current is total of the reverse leakage currents at PN junctions in the chip. This value is also extremely small at room temperature reaching only 1 nA (10^{-9} A) (standard value at Ta=25°C, V_{DD}=5V) for gate IC. Since this quiescent supply current is guaranteed over all possible combinations of logic conditions of input pins, the combinations will be of very

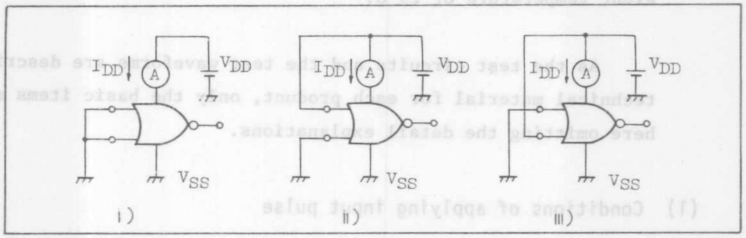


Fig. 1-18 Test Circuit of I_{DD}

large number and usually such quiescent supply current is guaranteed at the point where the distribution is higher than the actual situations taking a certain degree of margins for test precision and test method.

Fig. 1-18 illustrates examples of test circuits of I_{DD}. Since I_{DD} with both of two inputs holding "H" can be estimated by measuring at the conditions ii) and iii), the test is omitted in many cases.

(6) High level disable current/low level disable current (I_{DH}/I_{DL})

This item is not required for TC4001BP but it is required for the products having 3-state output and the products with open drain to specify the leakage current when the output is placed in the high impedance state.

I_{DH} is the leakage current when the signal of "H" level is applied to the OFF output and I_{DL} is the leakage current when the signal of "L" level is applie

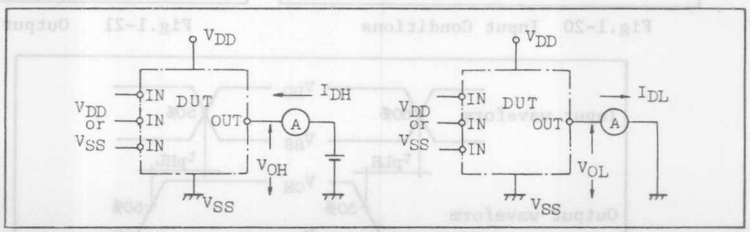


Fig. 1-19 Test Circuits of I_{DH}/I_{DL}

Fig. 1-19 illustrates the test circuits of disable current. Naturally, the inputs are connected to generate the high impedance state at the output to be measured.

5.2 Switching characteristics

The switching characterisiscs are to guarantee the transient characteristics of C^2MOS and specified with the load capacitance of 50pF at the ambient temperature of 25°C.

As the test circuits and the test waveforms are described in the technical material for each product, only the basic items are explained here omitting the detail explanations.

(1) Conditions of applying input pulse

Unless otherwise specified, pulse swinging completely from V_{SS} to V_{DD} shall be applied as the input waveform. The rise time and the fall time are the time required for the waveform to vary from 10% to 90%, and both of tr and tf are adjusted to 20ns. (Fig. 1-20)

(2) Output rise time/fall time (tr/tf)

The rise time and the fall time of output waveform are the time required for the waveform swinging from V_{OH} to V_{OL} to vary from 10% to 90%. (Fig. 1-21)

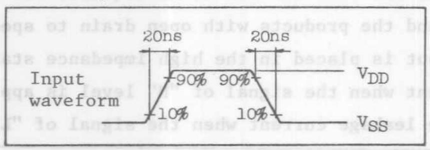


Fig.1-20 Input Conditions

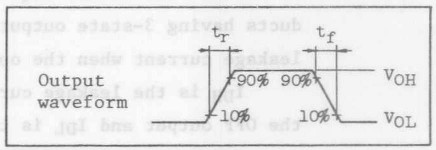
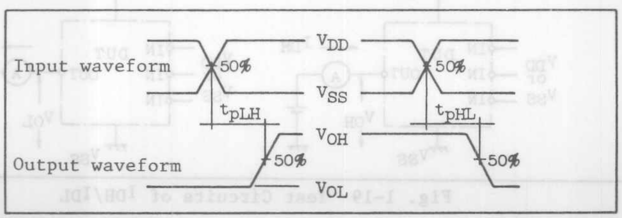


Fig.1-21 Output tr / tf



(3) High level propagation delay time/low level propagation delay time (t_{pLH}, t_{pHL})

These are the propagation delays from the time when signal is given to the input of IC being measured until the output responds. The time delay from varying the input level to the output to respond varying from "L" to "H" is called tpLH and on the contrary the time delay required for the output to vary from "H" to "L" is called tpHL. In practice, however, since the circuit threshold voltage of CMOS is $1/2 \cdot V_{DD}$ (theoretical value), the time delay is specified to be the time period between 50% point of the input waveform to 50% point of the output waveform.

It may be easy to understand concerning the gate ICs since the measurement conditions are less complicated, but MSI has higher number of input/output terminals and the delay time is specified designating the input pins and the output pins.

(4) Minimum pulse width (tw)

The counters and the registers have the clear and the preset inputs to determine the initial state in many cases.

The minimum pulse width is the critical value of pulse width with which these terminals recognize it as the normal signal, and since the maximum value of distribution is specified, it is required to apply pulse with the width wider than the value. The pulse width is specified by the time period between 50% point of the leading edge and 50% point of the trailing edge.

(5) Maximum frequency (maximum toggle frequency)

This is the maximum frequency at which the flip-flops and the counters perform normal operations, and the minimum value of distribution is specified. It is required to design applications with the condition of the minimum value or lower of the value specified.

Unless otherwise specified, the duty cycle of clock input is 50%.

(6) Maximum clock rise time/fall time (trø/tfø)

When the clock input waveform of a sequencial circuit, such as flip-flop or counter becomes dull, the possibility of racing or mis-counting (abnormal counting operations) arises. The critical values of trø and tfø are specified in the catalog and the clock inputs having rise time and fall time shorter than the minimum value are required.

(7) Data set-up time

The outputs of flip-flops and shift registers are determined by the conditions of data inputs at the time of clock input transition. Therefore, if the transitions of clock and data input occur at the same time, the output may not be definite, so that the data inputs require to be settled before the transition of clock input, and this required settling time is called data set-up time.

The maximum value of distribution is specified in the catalog and it is required to keep the set-up time longer than this value for applications.

〔2〕 INTRODUCTION AND BASIC APPLICATIONS OF PRODUCTS

[2] INTRODUCTION AND BASIC APPLICATIONS OF PRODUCTS

1. Gate/Buffer

Gate ICs are the fundamental ones of all the logic ICs, being used for switching applications with MSI and LSI. These devices are often independantly used as a square wave generating circuit, a one-shot pulse generating circuit. And in some cases it is composed of only gate ICs like a sequence control circuit. Anyhow, it is very important from the viewpoint of reduction in the quantity of parts used and of interface circuit design to know the versions of C^2MOS gate ICs.

In this chapter, therefore, the description of gate ICs shall be outlined before explaining applications of them.

1.1 Outline of gate/buffer

(1) Gate IC

Table 2-1 is a list of C^2MOS gates. In this table, simple one-stage gate systems (UB types) suitable to analog applications have been adopted as HEX INVERTER and QUAD 2-INPUT NAND/NOR gates, and three-stage gate systems (B types) have been adopted as switching elements for usual NAND gate and NOR gate.

A proper use of UB types and B types makes it possible to increase freedom on system design. These gate ICs can drive directly two low power TTL or one low lower Schottky TTL input.
However, since a standard TTL can not be directly connected, it must be driven by a buffer mentioned below.

(2) Buffer IC

Table 2-2 is a list of C^2MOS buffer gates. All the C^2MOS buffers can perform direct drive of one standard TTL input except P-channel open drain type.

Four types, TC4009UBP/TC4010BP/TC4049BP/TC4050BP, are provided with level converting function to drive the logic system of 5V (e.g., TTL/LSTTL) from CMOS of 5～18V (or other high voltage logic devices), in addition to applications of a usual buffer function.

Three versions, TC5012BP/TC5024BP/TC5025BP, are provided with 3-state outputs, permitting wired OR, which can be applied to the multiplexer or interface interface for bus lines and a usual system.

The open drain buffer has been developed for a logic level comvertor, a fluorescent display tube driver, etc.

Table 2-1 List of C^2MOS Gate

Function	Name	Logical Diagram	Circuit Configuration	DC Fan Out	Others
Inverter	TC4069UBP	×6		2 LTTL or 1 LSTTL Drivable	1-Stage Gate
NAND Gate	TC4011UBP	×4			
	TC4011BP TC7400BP				3-Stage Gate
	TC4023BP	×3			
	TC4012BP	×2			
	TC4068BP				
NOR Gate	TC4001UBP	×4			1-Stage Gate
	TC4001BP				3-Stage Gate
	TC4025BP	×3			
	TC4002BP	×2			
	TC4078BP				
AND Gate	TC4081BP				
	TC4073BP				
	TC4082BP				
OR Gate	TC4071BP				
	TC4075BP				
	TC4072BP				
EXCLUSIVE-OR Gate	TC4030BP				

List of C^2MOS Buffer

Function	Name	Logical Diagram	Equivalent Circuit	BC Fan Out	Others
Inverting Buffer	TC7404UBP	x6		1 TTL or 4 LSTTL Drivable	High to Low Level Conversion
	TC4009UBP				
	TC4049BP				
Non-inverting Buffer	TC4010BP	x6			
	TC4050BP				
3-State Buffer	TC5012BP	x6	Ø		3-State Outputs
	TC5024BP	x4	Ø		
	TC5025BP	x4	Ø		
Open Drain Buffer	TC5029BP	x4	V_{SS}		
	TC5064BP	x6	I_{NH} V_{DD}		(*) -50V
	TC5065BP	x6	I_{NH} V_{DD}		
	TC5066BP	x7	V_{DD}		
	TC5067BP	x7	V_{DD}		

Note) (*) Output Breakdown Voltage

(3) Multifunction Gate

In addition to the basic gates/buffers shown in Table 2-1 and Table 2-2, the C^2MOS family has three types of versions, that is, TC4019BP (Fig. 2-1) which selects 2-channel 4-bit data, TC4085BP (Fig. 2-2) containing two circuits which can be used as 2-channel data selector, and TC4086BP (Fig. 2-3) which can select 4-channel data.

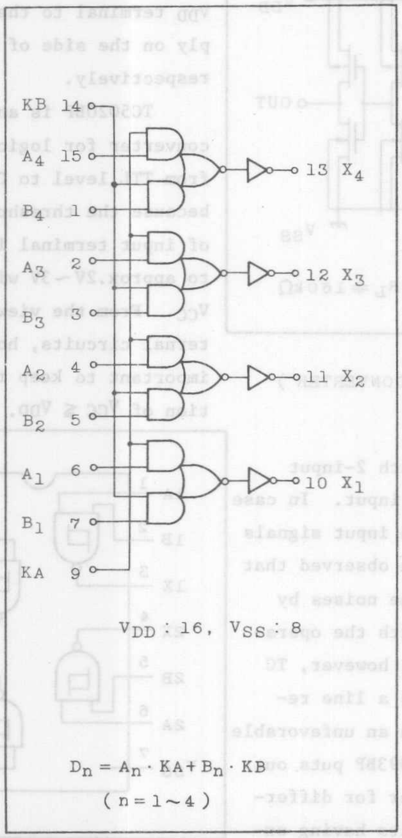


Fig. 2-1 TC4019BP
(QUAD AND-OR SELECT GATE)

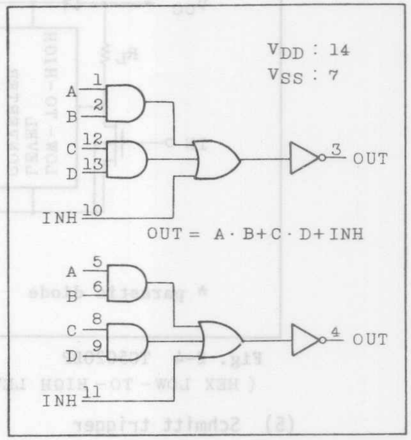


Fig. 2-2 TC4085BP
(DUAL 2 - WIDE 2 - INPUT AND / OR INVERT GATE)

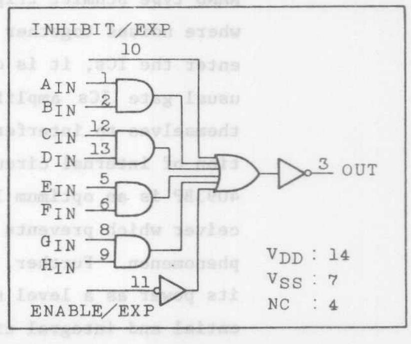


Fig.2-3 TC4086BP
(EXPANDABLE 4-WIDE 2-INPUT AND / OR INVERT GATE)

(4) Level converter

Further, the C^2MOS family has TC5020BP, a special logic level converter containing 6 circuits, which changes logic level of 5V, such as TTL/LSTT, to the logic level of 10V ~ 15V, such as C^2MOS. The equivalent circuit of TC5020BP is shown in Fig. 2-4.

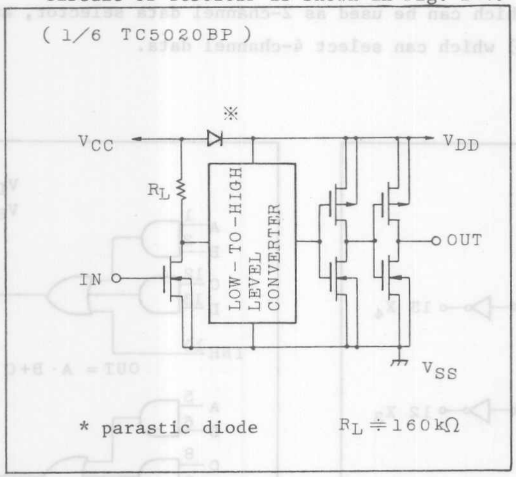


Fig. 2-4 TC5020BP
(HEX LOW-TO-HIGH LEVEL CONVERTER)

Usually a level converter is used by connecting V_{CC} terminal to the power supply on the side of low voltage, and V_{DD} terminal to the power supply on the side of high voltage, respectively.

TC5020BP is an ideal level converter for logic conversion from TTL level to CMOS level because the threshold voltage of input terminal is controlled to approx.2V ~ 3V without using V_{CC}. From the viewpoint of internal circuits, however, it is important to keep the condition of $V_{CC} \leqq V_{DD}$.

(5) Schmitt trigger

TC4093BP is a gate with 2-input NAND type Schmitt trigger input. In case where noises together with input signals enter the ICs, it is often observed that usual gate ICs amplify the noises by themselves to interfere with the operation of internal circuits; however, TC 4093BP is an optimum IC as a line receiver which prevents such an unfavorable phenomenon. Further, TC4093BP puts out its power as a level slicer for differential and integral circuits having extremely large time constants.

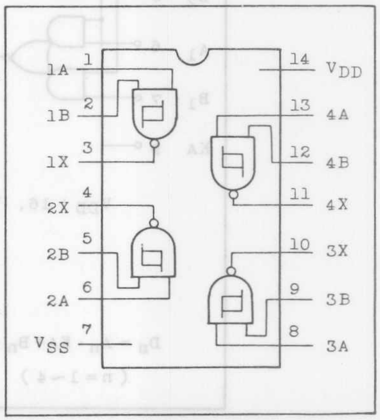


Fig. 2-6 TC4093BP
(QUAD 2-INPUT NAND SCHMITT TRIGGER)

TC4583BP is a 2-circuit Schmitt trigger, and outputs two-input exclusive OR in addition to forward output and inverse output.

TC4583BP consists of the circuits which generate input hysteresis voltage by inserting feedback resistors between POSITIVE/NEGATIVE and COMMON. Further the high level threshold voltage, low level threshold voltage, and hysteresis can be varied by changing these resistors. The threshold voltage can be varied within the range of hundreds of ohms through 100kΩ of external resistors.

The methods of connecting resistors are given in Fig.2-7. Fig.2-7 (a) shows a connecting method by use of one resistor, and Fig. 2-7 (b) shows a connecting method which the threshold voltages of high level and low level can be independently varied by using two resistors.

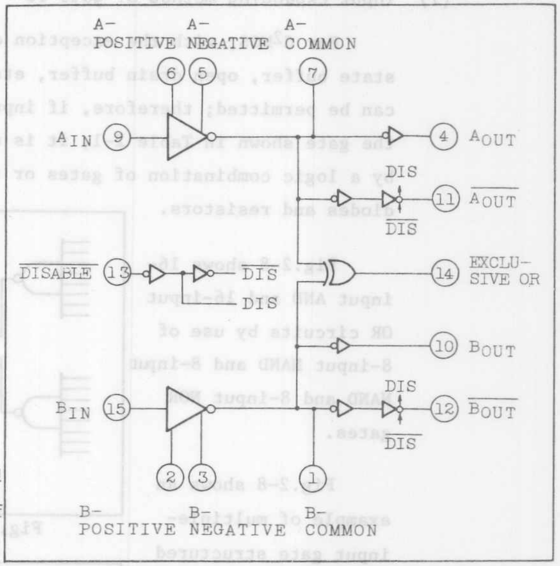


Fig. 2-6 TC4583BP Dual Schmitt Trigger

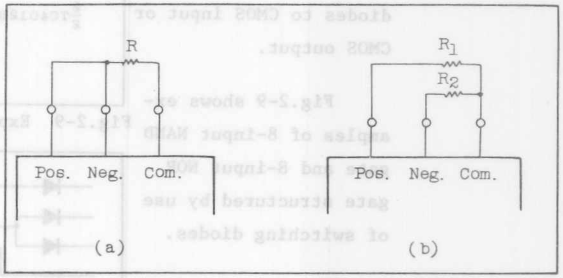


Fig. 2-7 TC4583BP Method of Connecting Resistors for V_H Reguration

1.2 Application of gate IC

(1) Input expanding method of gate IC

For C^2MOS, with the exception of special cases of connecting 3-state buffer, open drain buffer, etc., no direct connection between outputs can be permitted; therefore, if input has become insufficient by use of the gate shown in Table 2-1, it is necessary to make a mutiple-input gate by a logic combination of gates or to structure AND and OR by use of diodes and resistors.

Fig.2-8 shows 16-input AND and 16-input OR circuits by use of 8-input NAND and 8-input NAND and 8-input NOR gates.

Fig.2-8 shows an example of multiple-input gate structured by a combination of gates. In addition, there is a method which a wired OR can be realized by connecting diodes to CMOS input or CMOS output.

Fig.2-9 shows examples of 8-input NAND gate and 8-input NOR gate structured by use of switching diodes.

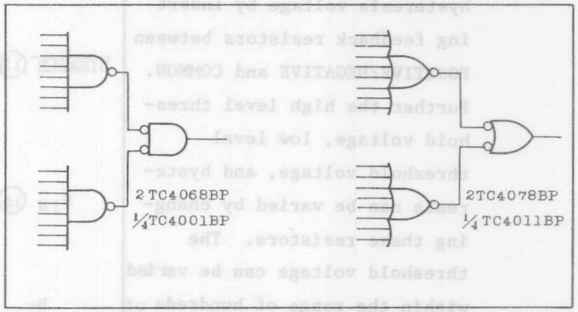


Fig. 2-8 Input AND/OR Gates

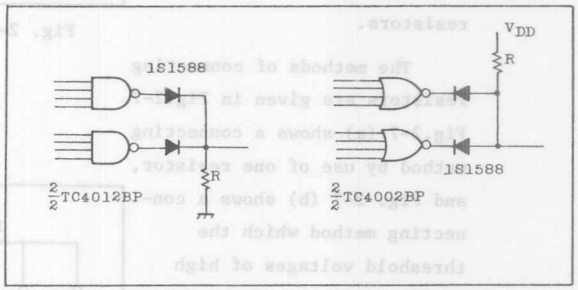


Fig.2-9 Expansion of Gate by Diodes and Resistors (1)

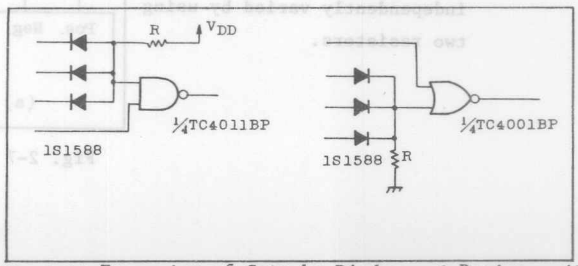


Fig.2-10 Expansion of Gate by Diodes and Resistors(2)

Fig. 2-10 shows a method of increasing inputs in number by use of diodes in the same way. In case of the gate expnasion methods by use of diodes and resistors illustrated in Fig. 2-9 and Fig. 2-10, care should be exerted to time the current drives because the diode gates themselves have no amplification function. Since the resistance value R must be sufficiently large as compared with output impedance of CMOS and must be so small that the level variation may not be caused by induction or the like, it is recommended that usually the resistance value be approx. 10 kΩ ~ 1MΩ.

With this diode gate system, high level signal line voltage is $V_{OH} - V_F$ (V_F denotes diode forward voltage) and low level signal line voltage is $V_{OL} + V_F$, resulting in a reduction of noise immunity further direct current flows in the resistors. Therefore, this system should not be used with extraordinary frequency, by it should be applied when the increase in package is prevented at time of shortage of one gate only or when some gate outputs are not sufficient in number.

(2) Pulse delay circuit and hazard absorption circuit

Pulse phase is relatively often delayed on a logical circuit, and this circuit is generally often made up by inserting capacitors into the signal lines. With C^2MOS IC, a fairly long period of delay can be obtained by using CR because input impedance is extremely high. Fig. 2-11 shows the basic delay circuit of C^2MOS IC. In this figure, the input waveform can be integrated by R_T and C_T inserted into the circuit (Waveform Va). When this integrated waveform is sliced by the circuit threshold value (V_{TH2}) of the inverter ②, resultantly the waveform appears on the output as a waveform being later by t_{pd2} in rising time than the input waveform.

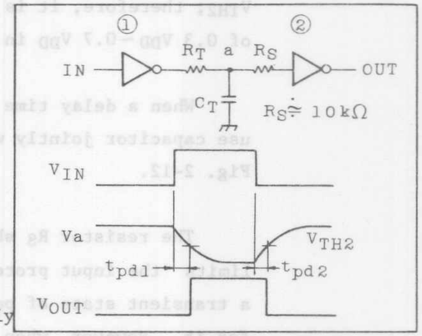


Fig. 2-11 Pulse Delay Circuit

This delay time is shown in the following formulas by ingoring the internal delay of IC.

$$t_{pd1} = -R_T C_T \cdot \ell n \left(\frac{V_{TH2}}{V_{DD}}\right) \text{ .... (S)} \quad \text{..... (2.1)}$$

$$t_{pd2} = -R_T C_T \cdot \ell n \left(\frac{V_{DD}-V_{TH2}}{V_{DD}}\right) \text{ ...... (S)} \quad \text{..... (2.2)}$$

R_T ; [Ω] C_T ; [F]

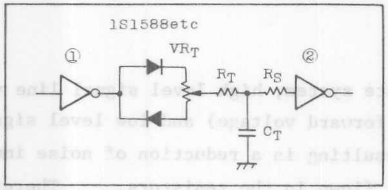


Fig.2-12 Delay Time Regulating Circuit

And, let V_{TH2} be an ideal state of $1/2V_{DD}$, the delay time is determined by the expression $t_{pd1} = t_{pd2} = 0.69\ C_T R_T$. Actually, however, when TC4049BP (TC4001BP or TC4011BP may be used as inverter) is used as an inverter, there may be a variation of $0.3\ V_{DD} \sim 0.7\ V_{DD}$ in V_{TH2}; therefore, it is necessary to recognize that there is a variation of $0.3\ V_{DD} \sim 0.7\ V_{DD}$ in both t_{pd1} and t_{pd2}.

When a delay time is required to be defined, it is desirable to use capacitor jointly with vatiable resistors, for example, as shown is Fig. 2-12.

The resistor R_S shown in Fig. 2-11 or Fig. 2-12 is a resistor which limits the input protected diode forward current of the inverter ② in a transient state of power supply; therefore, approx. 10 kΩ is sufficient for it. However, when C_T is less than 500pF, and when the inverter ② is TC4049BP, this resister can be eliminated. Since the register R_T used for deciding time constant is considerably affected by the output impedance of inverter ① being small value, it may be said to be satisfactory that its registance is 10kΩ ~10MΩ.

For this type of delay circuit, since the inverter ② slices the waveform which makes a slow change, the output edge may be apt to oscillated by the influence of power supply ripples. This effect becomes remarkable when the time constant of $C_T R_T$ is especially large, so that mulfunction may be considered when the output of inverter ② has been connected to the clock input of counter F/F or the like.

It is effective that the inverter ② is repalced with Schmitt trigger gate to prevent such mulfunction.

To return to the circuit shown in Fig. 2-11, since the potential of point "a" cannot vary up to V_{TH2} when the signal of pulse width of less than 0.36 $C_T R_T$ has been applied to this circuit, the output does not invert; therefore, the potential can be used as hazard killer or noise killer.

(3) Schmitt trigger circuit

When the inverters (NAND gate and NOR gate) are connected each other in series, and positive feedback is applied to them by using proper resistor (R_f) (Shown in Fig.2-13) it becomes possible to make up Schmitt trigger circuit, which provides hysteresis to the input threshold voltage.

Fig. 2-13 shows Schmitt trigger circuit in which two inverters and two resistors are used. With this circuit, the inverted voltage of the circuit seen from the input terminal side becomes V_P at rise time and V_N at fall time, resulting in having the hysteresis voltage equivalently shown in the following equation:

$$V_H = V_P - V_N \qquad \text{............ (2.31)}$$

High level threshold voltage (V_p) and low level threshold voltage (V_N) are expressed as follows:

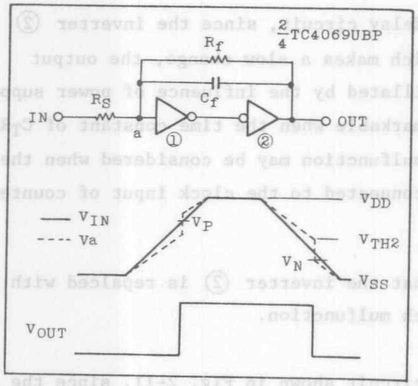


Fig. 2-13 Schmitt Trigger Circuit

$$V_P = \left(\frac{R_S + R_f}{R_f}\right) V_{TH} \quad \ldots (2.3)$$

$$V_N = \left(\frac{R_S + R_f}{R_f}\right) V_{TH} - \left(\frac{R_S}{R_f}\right) V_{DD} \quad (2.4)$$

Therefore, the hysteresis voltage V_H is then from the formulas of (2.31), (2.32) and (2.4).

$$V_H = \left(\frac{R_S}{R_f}\right) V_{DD} \quad \ldots\ldots\ldots\ldots (2.5)$$

Here, it is assumed that R_f is sufficently large as compared with the output impedance of the inverter ②. The theoretical values of V_P, and V_N in this case are shown in Fig. 2-14 and Fig. 2-15.

For these figures, full consideration is given to the fact that V_{TH2} has shifted from 0.3 V_{DD} up to 0.7 V_{DD}. In case of this type of Schmitt trigger circuit as clearly shown in the same figures, the impedances should be used under the condition, $R_S/R_f \leqq 0.4$, which shows that it is difficult to expect V_H of more than 0.4V_{DD}.

And, in case of Fig. 2-13 the input impedance is as follows:

$$R_{IN} \fallingdotseq R_S + R_f$$

Therefore, when the inverter is connected to the signal source impedance being very higher than R_{IN}, normal operation may not be expected.

In Fig. 2-13, the feedback capacitor inserted, in parallel, in the feedback resistor R_f is used for improving the phase of positive feedback by the inverter ② ; therefore, its ideal value is approx. 500pF.

Since TC4093BP in Fig. 2-5 and TC4583BP in Fig. 2-6 shown in 1.1(5) of this chapter are Schmitt trigger IC equipped with general CMOS inputs, connection can be connected with no trouble even when the signal source impedance is high. For practical circuits, it is important to adapt which device in responce to applications and case by case.

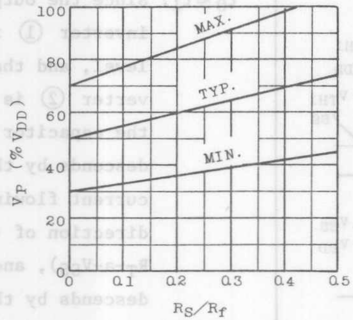


Fig.2-14 R_S/R_f-V_P
(Theoretical Value)

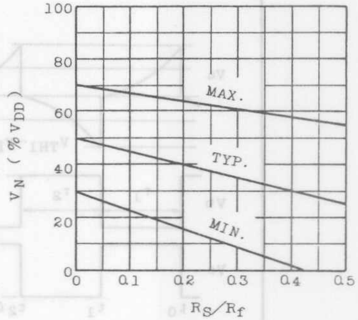


Fig.2-15 R_S/R_f-V_N
(Theoretical Value)

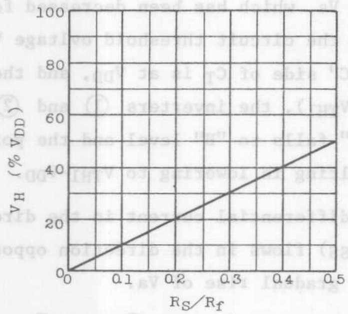


Fig.2-16 R_S/R_f-V_H
(Theoretical Value)

(4) Astable multivibrator

The astable multivibrator may be called a square waveform oscillator circuit in other words, being generally used for the following applications:

a) Clock pulse generating source of electronic equipment

b) Time base of timer, etc.

Fig. 2-17 shows the principle diagram of an astable multivibrator by two stages of CMOS inverters. (For analyzing the circuit, the effect by the input protection circuit of the inverter 1 shall not be considered.)

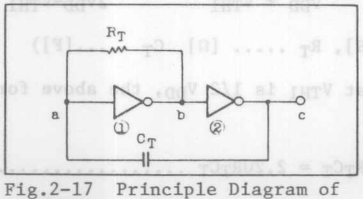


Fig.2-17 Principle Diagram of CMOS Astable Multivibrator

Fig. 2-18 shows the voltage waveform of each portion of the circuit in Fig. 2-17. Now, conceive each time of t_0, t_1 and t_2 in Fig. 2-18, and let us think of the operation of circuit at each time.

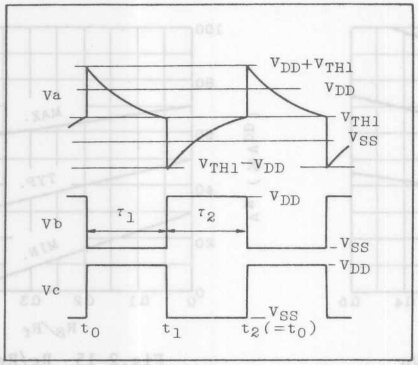


Fig. 2-18 Voltage Waveform of Each Portion

$t_0 \sim t_1$: Since the output of the inverter ① is at "L" level, and that of the inverter ② is at "H" level, the capacitor C_T gradually descends by the differential current flowing in the direction of (V_{DD}-C-C_T-a R_T-a-V_{SS}), and Va gradually descends by the time constant decided by $C_T R_T$, respectively.

t_1 : When the potential Va, which has been decreased for the period of $t_0 \sim t_1$, reaches the circuit threshold ovltage V_{TH1} (in which the potential on "C" side of C_T is at V_{DD}, and the potential on "a" side is at V_{TH1}), the inverters ① and ② inverter, by which the point "b" falls to "H" level and the point "c" falls to "L" level, resulting in lowering to V_{TH1}-V_{DD}.

$t_1 \sim t_2$: In this case, the differential current in the direction of (V_{DD}-C-C_T-a-R_T-b-V_{SS}) flows in the direction opposite to $t_0 \sim t_1$, resulting in a gradual rise of Va.

t_2 : When Va reaches V_{TH1}, the inverters ① and ② reinvert, which raises Va to V_{DD} + V_{TH1}. This mode is the same as t_1.

Like this, the circuit in Fig. 2-17 continues oscillation in a cycle constantly determined by the time constants of C_T and R_T.

The oscillation cycle T of this circuit is expressed by the following equation:

$$T = \zeta_1 + \zeta_2 = -R_T C_T \left[\ell n \left(\frac{V_{TH1}}{V_{DD} + V_{TH1}}\right) + \ell n \left(\frac{V_{DD} - V_{TH1}}{2V_{DD} - V_{TH1}}\right)\right] \quad ....(2.6)$$

(T, ζ_1, ζ_2 .....[S], R_T ..... [Ω], C_T .....[F])

where, if it is assumed that V_{TH1} is 1/2 V_{DD}, the above formula becomes the following equation:

$$T(0.5) = 1.1R_T C_T + 1.1R_T C_T = 2.20R_T C_T \quad .... (2.7)$$

Even if the worst cases where V_{TH1} is $0.7V_{DD}$ and $0.3V_{DD}$, are considered, they are as follows:

$$T(0.7) = 0.887R_TC_T + 1.466R_TC_T = 2.35R_TC_T$$

$$T(0.3) = 1.466R_TC_T + 0.887R_TC_T = 2.35R_TC_T$$

Theoretically, even if V_{TH1} deflects in any direction from 1/2 V_{DD}, the cycle T is 106.8% against T(0.5) at the worst, though it is, more or less, prolonged. Namely, the oscillation cycle is the sum of differentiation on the plus side and that on minus side, so that if one side makes change, another one shifts in the direction of offsetting the changed portion. As the result, the oscillation waveform of relatively stable cycle can be expected. Fig. 2-19 shows the regulation of V_{TH1} and oscillation cycle.

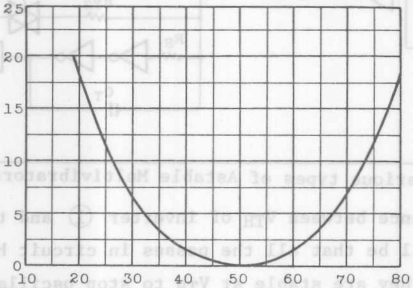


Fig. 2-19 Regulation by V_{TH} of Oscillation Cycle

In order to make up this astable multivibrator by using actual C^2MOS IC, it is necessary that the input protection diode of the inverter ① omitted in Fig.2-17 is taken into consideration. In other words, the potential of Va in Fig. 2-18 exceeds cyclically the input rating of inverter ① on both pluse and minus sides, therefore, it is necessary to insert the current limit resistor R_S between the point "a" and the inverter ① input. When this R_S is made small, the oscillation cycle T becomes smaller than the theoretic value on circuit operation; therefore, it may be said that this R_S should be selected under the conditions of $R_S > 2R_T$.

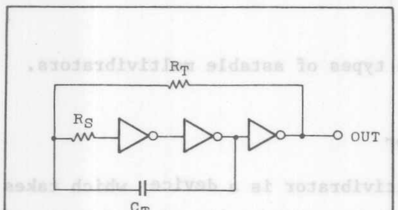


Fig. 2-20 Astable Multivibrator of Oscillation Stability Type

With the circuit in which the two stages of inverter in Fig.2-7 is used, the input and output of the inverter ① become connected by resistors.

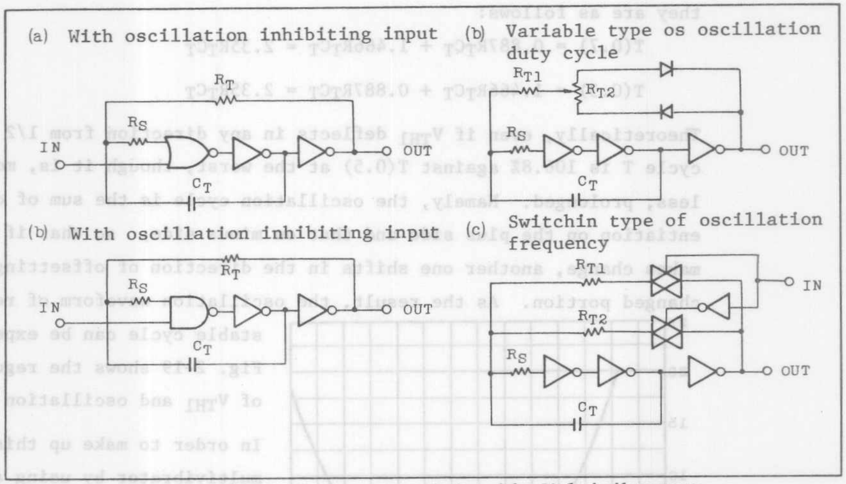


Fig. 2-21 Various types of Astable Multivibrators

If there is no difference between V_{TH} of inverter ① and that of inverter ②, it may well be that all the passes in circuit have the stability point where they are stable at V_{TH} to stop oscillation. When the circuit in Fig. 2-17 is, in reality, combined with CMOS IC, such a state is sometimes brought about by a combination of capacitor C_T and resistor R_T.

Thus, it is recommended from the point of stability in oscillation that the method of using the circuit with three inverters as shown in Fig. 2-20 be adopted.

Fig. 2-21 shows various types of astable multivibrators.

(5) Monostable multivibrator

The monostable multivibrator is a device which takes out the pulse output of necessary width by catching the edge of logic signal at rise or fall time. This device is widely used in a pulse stretcher, which stretches pulse waveform with narrow width, and for making a long signal pulse into a trigger pulse.

Fig. 2-22 shows the basic circuit of monostable multivibrator (hereinafter it is called "monomulti" for short). In this example, as TC4001BP is used, the pulse of positive polarity can be obtained for the output at the rise time of input pulse.

The output pulse width is determined by the time constants of C_T and R_T, and the following equation is obtained

$$Va=V_{DD}(1-EXP(-\frac{t}{R_TC_T}))$$

from the above formula, the formula "a" is indued as follows:

$$t=-R_TC_T\cdot \ell n\ (1-\frac{Va}{V_{DD}})$$

Therefore, the output pulse width can be expressed by means of the following formula:

$$t_W=-R_TC_T\cdot \ell n(1-\frac{V_{TH2}}{V_{DD}})\ ..(2.8)$$

(V_{TH2}: Device threshold voltage of inverter 2).

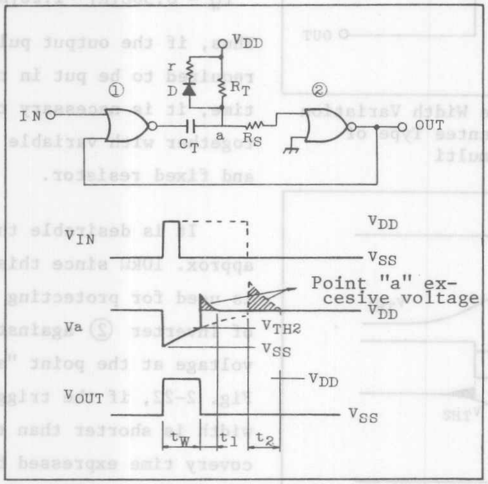


Fig. 2-22 Basic Circuit of Monostable Multivibrators

Here, let V_{TH2} = 1/2 V_{DD}, we can obtain

$$t_W = 0.69C_TR_T$$

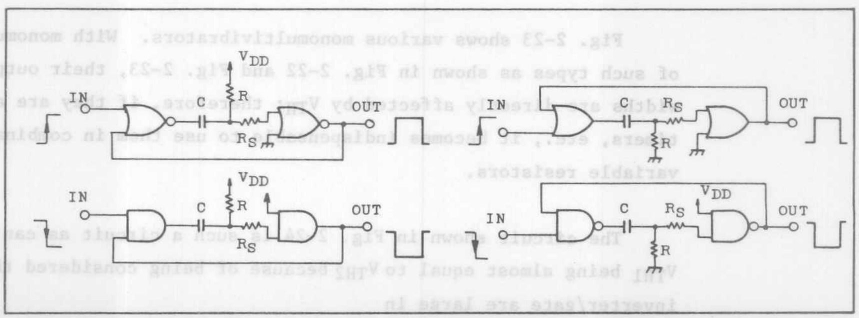


Fig. 2-23 Various Types of Monostable Multivibrators

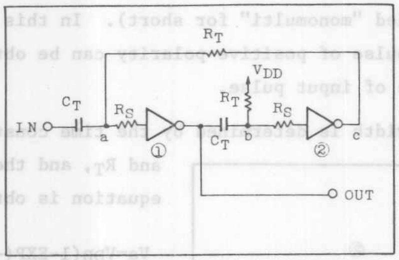


Fig. 2-24 Pulse Width Variation Guarantee Type of Monomulti

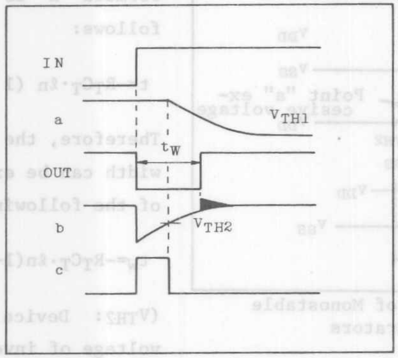


Fig. 2-25 Voltage Waveform of Each Portion

If V_{TH2} varies to the worst level of $0.3V_{DD} \sim 0.7V_{DD}$, it varies within the range of the following equation:

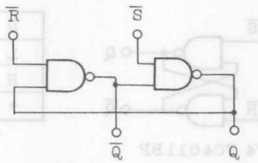
$$t_W = 0.36C_TR_T \sim 1.2C_TR_T$$

Thus, if the output pulse width is required to be put in the defined time, it is necessary to use R_T together with variable resistor and fixed resistor.

It is desirable that R_S is approx. 10kΩ since this resistor is used for protecting the input of inverter ② against excessive voltage at the point "a". In Fig. 2-22, if the trigger pulse width is shorter than t_W, the recovery time expressed by t_1 is required, and if it is longer than t_W, the recovery time expressed by t_2 is required. Therefore, when this recovery time is required to be made shorter, the speed-up circuits ($r \geqq 500\Omega$) expressed by D and r in Fig. 2-22 should be inserted into the monovibrator.

Fig. 2-23 shows various monomultivibrators. With monomultivibrators of such types as shown in Fig. 2-22 and Fig. 2-23, their output pulse widths are directly affected by V_{TH}; therefore, if they are applied to timers, etc., it becomes indispensable to use them in combination with variable resistors.

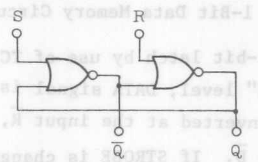
The circuit shown in Fig. 2-24 is such a circuit as can utilize V_{TH1} being almost equal to V_{TH2} because of being considered that C^2MOS inverter/gate are large in



$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
L	L	H	H
L	H	L	H
H	L	H	L
H	H	Q*	$\overline{Q}$*

* HOLD

TC4011BP



R	S	Q	$\overline{Q}$
L	L	Q*	$\overline{Q}$*
L	H	H	L
H	L	L	H
H	H	L	L

* HOLD

TC4001BP

Fig. 2-26 R-S Flip-Flops

variation in threshold values between packages, but the variation in V_{TH} within the same package can be held down to $2 \sim 3\%$. Therefore, if $V_{TH1} \fallingdotseq V_{TH2} = V_{TH}$, the output pulse width t_W can be expressed by the following formula:

$$t_W = -R_T C_T \left[\ln\left(\frac{V_{DD}-V_{TH}}{V_{DD}}\right) + \ln\left(\frac{V_{TH}}{V_{DD}}\right) \right] \text{ .... (2.9)}$$

in which if $V_{TH}=1/2V_{DD}$, $t_W=1.38R_TC_T$,
and if $V_{TH}=0.3V_{DD}$ or $0.7V_{DD}$, $t_W=1.55R_TC_T$

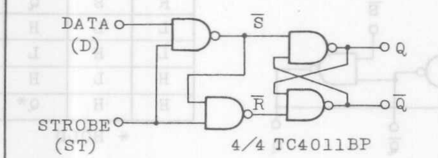
Thus, even in case of the worst level, the scatter can be held down by the increase of 12% of the minimum value.

(6) Bistable multivibrator (Flip-flop)

The bistable multivibrator will be explained in details in [2]4, but here as the example of flip-flop configurated by use of gate IC its basic circuits only illustrates. Fig.2-26 shows R-S flip-flop for which NAND gate TC4011BP and NOR gate TC4001BP have been used.

The flip-flop of this shape is extremely often applied to control circuits, etc.

(7) Latch circuit

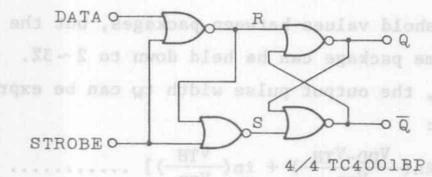


D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
*	L	Q_n ·	$\overline{Q_n}$ ·

* Don't care
· Hold

Fig. 2-29 1-Bit Data Memory Circuit (1)

Fig. 2-29 shows the 1-bit latch by use of TC4011BP. With this circuit, when STROBE is at "H" level, DATA signal is inverted at the input $\overline{S}$ of R-S flip-flop and noninverted at the input $\overline{R}$, so that this circuit shows the state of Q = D and $\overline{Q} = \overline{D}$. If STROBE is changed from "H" level to "L" level in this state, both $\overline{S}$ and $\overline{R}$ reach "H" level, and R-S flip-flop holds DATA at STROBE fall time.



D	ST	Q	$\overline{Q}$
L	L	L	H
H	L	H	L
*	H	Q_n ·	$\overline{Q_n}$ ·

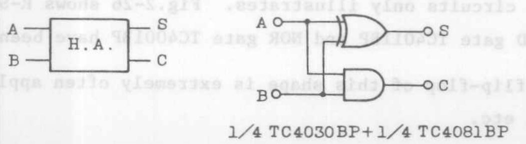
* Don't care
· Hold

Fig. 2-30 1-Bit Data Memory Circuit (2)

Fig. 2-30 shows the 1-bit latch by use of TC4001BP, in which the STROBE logic becomes contrary to that shown in Fig. 2-29.

Each circuit in Fig. 2-29 and Fig. 2-30 is 1-bit circuit, but it is recommended that TC4042BP (4 BIT D-LATCH), TC4508BP (DUAL 4 BIT D-LATCH) or the like be used for processing the data of 4 bits or more.

(8) Foundation of operation circuit

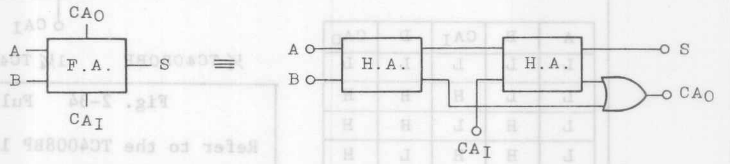


A	B	S	C
L	L	L	L
L	H	H	L
H	L	H	L
H	H	L	H

Fig. 2-31 Half Adder

Fig. 2-31 shows a basic half-adder, and the logical expression of SUM and CARRY outputs is as follows:

$$S = A \oplus B, \quad \text{and } C = A \cdot B$$



A	B	CA_I	S	CA_O
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Fig. 2-32 Full Adder

Fig.2-32 shows a full adder which is provided with both carry function from lower order and carry output to higher order.

The logical expressions of S and CA_O are as follows:

$$S = (A \oplus B) + CA_I \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2.10)$$

$$CA_O = A \cdot B + (A \oplus B) \cdot CA_I \quad \ldots\ldots\ldots\ldots\ldots \quad (2.11)$$

Basically,the addition of binary n-bits can be realized by connecting n-units of this full adder.

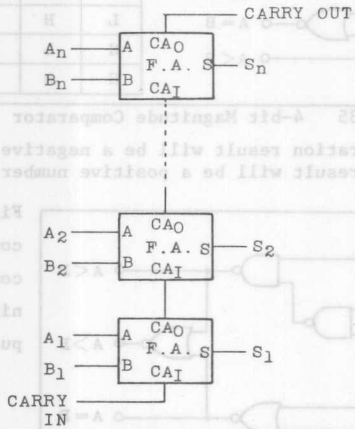
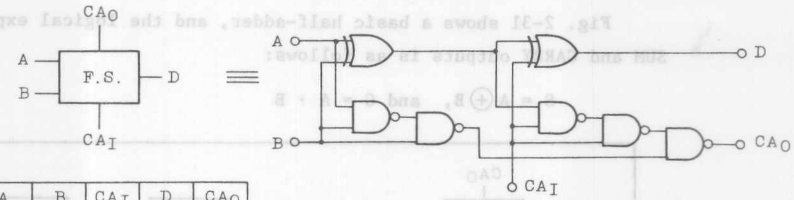


Fig. 2-33 N-bit Parallel Adding Circuit

Fig.2-33 shows a basic parallel adder of n-bits. Since the add time in this circuit is delayed as the CARRY signal holds higher-order position, it is decided by this delay time, resulting in disadvantage to high-speed operation. Therefore, for an ordinary binary adder (e.g., TC4008BP of C^2MOS IC), such a method as carry out is generated by taking CARRY signal only in advance is often chosen.

This method is followed by using LOOK AHEAD CARRY CIRCUIT.



A	B	CA_I	D	CA_O
L	L	L	L	L
L	L	H	H	H
L	H	L	H	H
L	H	H	L	H
H	L	L	H	L
H	L	H	L	L
H	H	L	L	L
H	H	H	H	H

¼ TC4030BP   1¼ TC4011UBP

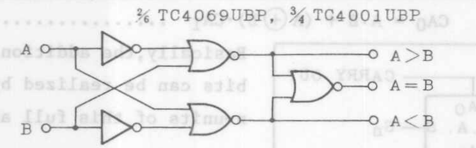
Fig. 2-34   Full Subtractor

Refer to the TC4008BP logical circuits of individual technical material which are not described in this chapter, if you take an interest in this field.

Fig.2-34 shows an example of full subtractor. In the same figure, the input A denotes minuend, the input B denotes subtrahend, CA_I denotes borrow input from higher order, and CA_O denotes borrow output to higher order,respectively.

Binary subtract circuit of n-bits can be structured by connecting full subtractors each other in the same way as shown in Fig.2-33. In this case,

⅔ TC4069UBP, ¾ TC4001UBP

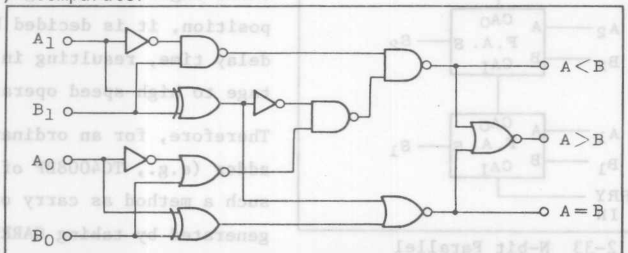


A	B	A>B	A=B	A<B
L	L	L	H	L
L	H	L	L	H
H	L	H	L	L
H	H	L	H	L

Fig. 2-35   4-bit Magnitude Comparator

if CARRY OUT is "H", operation result will be a negative number, and if it is "L", the operation result will be a positive number.

(9) Comparator



¾ TC4030BP, ¾ TC4011UBP, ¾ TC4001UBP
⅚ TC4069UBP

Fig. 2-36   2-bit Magnitude Comparator

Fig.2-35 shows a comparator which compares the magnitude of two inputs, voltage A and B.

Fig.2-36 shows a magnitude comparator which detects the magnitude or coincidence of data inputs (A) and (B) of 2 bits.

For detecting the magnitude of data (BCD or Binary) of more than 4 bits, it is advisable to use TC4585BP or TC4063BP of C^2MOS MSI.

Fig. 2-35 and Fig. 36 show comparators which can decide the magnitude and coincidence of inputs. If coincidence only is required, the identity unit shown in Fig.2-37 is used. In Fig.2-37, only when the data of [A] and [B] have coincided each other, the output is at "H" level; for other modes, the output is at "L" level.

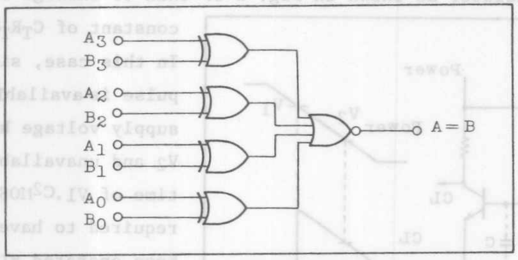


Fig. 2-37 4-bit Coincidence Circuit

(10) Auto reset initialized circuit

Generally, for an electronic circuit, it is often required to initialize the circuit when the power is turned on. Specially, for the counter, flip-flop,etc,. the initialization is established by temporarily making CLEAR terminals active when the power is turned on; because it is uncertain whether output is turned to "H" level or "L" level when the power supply has applied to them.

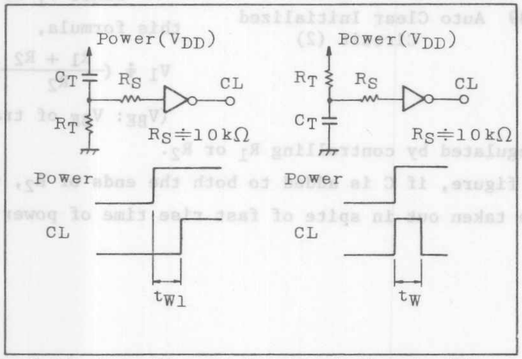


Fig.2-38 Auto Clear Initialized Circuit (1)

Fig. 2-38 shows the circuits to be used at time of relatively sharp rise of the power supply. If the rise power supply is of step-like waveform, the output pulse width can be calculated by the following eauations:

$$t_{W1} = -R_T C_T \cdot \ln \frac{V_{TH}}{V_{DD}} \qquad \text{....... (2.12)}$$

$$t_{W2} = -R_T C_T \cdot \ln (1- \frac{V_{TH}}{V_{DD}}) \qquad \text{....... (2.13)}$$

For this circuit, however, the rise time of power supply should be short enough as compared with t_W.

On the contrary, in case of delay in rise time of power supply, it is more advantageous to make up the circuit by use of three resistors and one transistor as shown in Fig. 2-39 than to enlarge the time constant of $C_T R_T$.

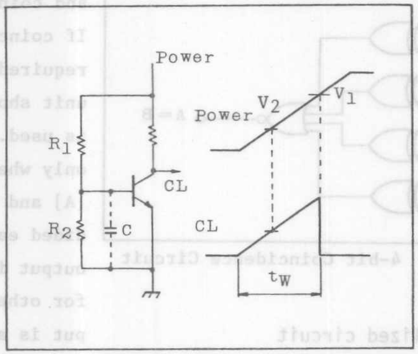


Fig. 2-39 Auto Clear Initialized Circuit (2)

In this case, since clear pulse is available when the supply voltage has become V_2 and unavailable at the time of V_1, C^2MOS circuit is required to have already been operated at the time of V_1. Then R_1 and R_2 are set at proper values.

Since V_1 is expressed by this formula,

$$V_1 \doteqdot \left(\frac{R_1 + R_2}{R_2}\right) V_{BE}$$

(V_{BE}: V_{BE} of transistor),

V_1 can be regulated by controlling R_1 or R_2.

In the same figure, if C is added to both the ends of R_2, the output pulse can be taken out in spite of fast rise time of power supply.

2. Decoder/Encoder

The decoder is a code converter which decodes such code signals as binary signal and binary coded decimal (BCD) signal, to such signals as N signal and decimal signal.

There are various applications in an actual system, including a decoder which converts the BCD code to the 7-segment desplay driving signal.

An encoder is a code converter which converts the signals, such as N signal and decimal signal, to the code signals, such as binary signal and binary coded decimal signal.

Since various decoders are available in the C^2MOS family, it is advisable to use them properly.

2.1 Outline of decoder/encoder

Table 2-3 List of C^2MOS Decoder/Encoder

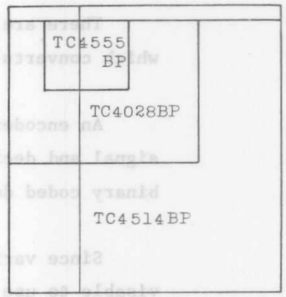
Function		Name of Products
Binary — N	Binary — Quadrinary	TC4555BP, TC4556BP
	Binary — Octal	TC4028BP
	Binary — Hexadecimal	TC4514BP, TC4515BP
BCD — Decimal		TC4028BP
BCD — 7-segment	LED DRIVE	TC4511BP, TC5002BP TC5022BP,
	LCD DRIVE	TC4055BP, TC4056BP, TC4543BP
N — Binary	Octal — Binary	TC4532BP

Table 2-3 shows Decoder/Encoder of C^2MOS.

Table 2-4 C²MOS Decoder Truth Table

a) C²MOS Decoder Truth Table ("H" level output)

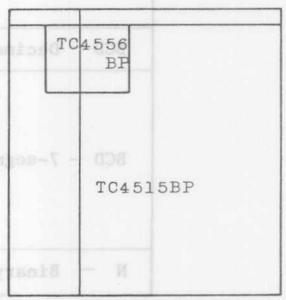
INPUTS				OUTPUTS															
D	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}
L	L	L	L	H															
L	L	L	H		H														
L	L	H	L			H													
L	L	H	H				H												
L	H	L	L					H											
L	H	L	H						H										
L	H	H	L							H									
L	H	H	H								H								
H	L	L	L									H							
H	L	L	H										H						
H	L	H	L											H					
H	L	H	H												H				
H	H	L	L													H			
H	H	L	H														H		
H	H	H	L															H	
H	H	H	H																H



* All blank columns are for "L".

b) C²MOS Decoder Truth Table ("H" level output)

INPUTS				OUTPUTS															
D	C	B	A	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$	$\overline{Q_6}$	$\overline{Q_7}$	$\overline{Q_8}$	$\overline{Q_9}$	$\overline{Q_{10}}$	$\overline{Q_{11}}$	$\overline{Q_{12}}$	$\overline{Q_{13}}$	$\overline{Q_{14}}$	$\overline{Q_{15}}$
L	L	L	L	L															
L	L	L	H		L														
L	L	H	L			L													
L	L	H	H				L												
L	H	L	L					L											
L	H	L	H						L										
L	H	H	L							L									
L	H	H	H								L								
H	L	L	L									L							
H	L	L	H										L						
H	L	H	L											L					
H	L	H	H												L				
H	H	L	L													L			
H	H	L	H														L		
H	H	H	L															L	
H	H	H	H																L



* All blank columns are for "H".

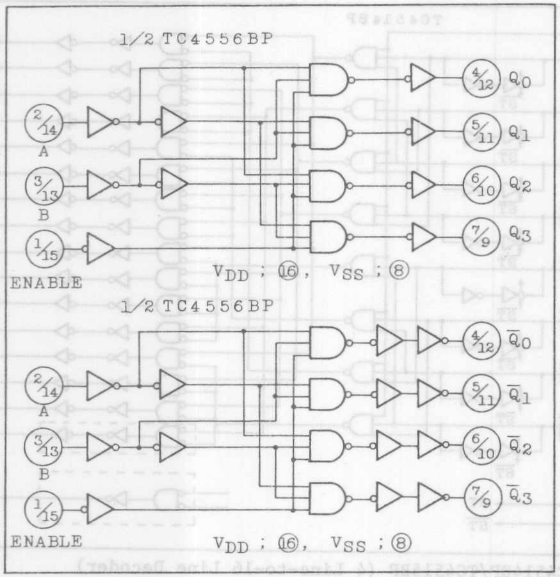


Fig. 2-40 TC4555BP/TC4556BP (Dual Binary-to-10F4 Decoder)

(1) Binary-N-nary and BCD-decimal decoder

The truth table of Binary — N-decoder is shown in Table 2-4. The output selected by means of a binary code input appears at "H" level or "L" level.

TC4555BP and TC4556BP are the binary to quadrinary decoder with two circuits, and have function capable of inhibiting selection by setting ENABLE input to "H" level. The logic diagrams of TC4555BP and TC·45556BP are shown in Fig. 2-40.

TC4028BP is a BCD - decimal decoder, and its output is selcted at "H" level. If the input D of TC4028BP is set to "L" level, this device can be used as an octal decoder from a binary code of 3 bits of ABC. In this case, if the input D is set to "H" level, it can be used as INHIBIT input becsuse all of $Q_0 \sim Q_7$ are at "L" level.

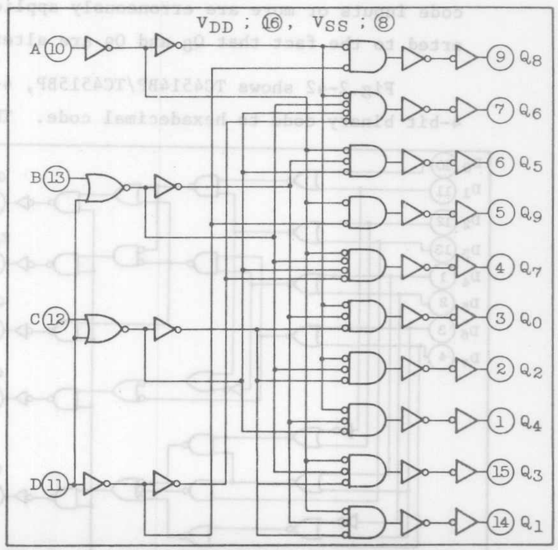


Fig.2-41 TC4028BP (BCD-to-Binary Decoder)

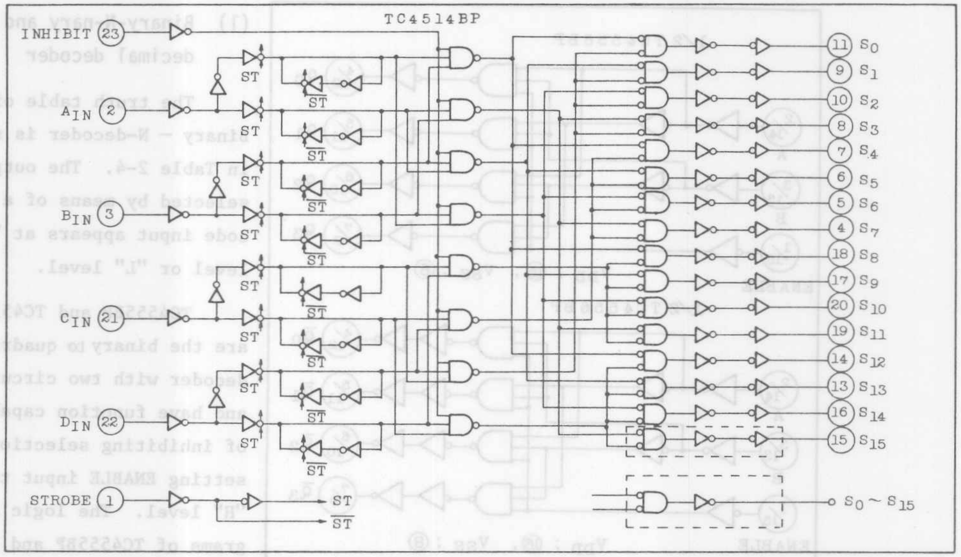
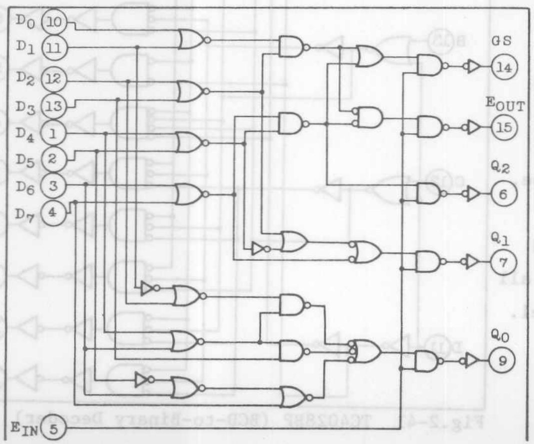


Fig. 2-42 TC4514BP/TC4515BP (4 Line-to-16 Line Decoder)

Since the decode of TC4028BP is not of a full decoding type, if ten binary code inputs or more are erroneously applied to this decoder, care should be exerted to the fact that Q_8 and Q_9 are alternately set at "H" level.

Fig.2-42 shows TC4514BP/TC4515BP, 4-to-16 Line Decoders, which convert 4-bit binary code to hexadecimal code. The output of TC4515BP is selected to



INPUT									OUTPUT				
E_{IN}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	GS	Q_2	Q_1	Q_0	E_{OUT}
L	※	※	※	※	※	※	※	※	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	※	※	※	※	※	※	※	H	H	H	H	L
H	L	H	※	※	※	※	※	※	H	H	H	L	L
H	L	L	H	※	※	※	※	※	H	H	L	H	L
H	L	L	L	H	※	※	※	※	H	H	L	L	L
H	L	L	L	L	H	※	※	※	H	L	H	H	L
H	L	L	L	L	L	H	※	※	H	L	H	L	L
H	L	L	L	L	L	L	H	※	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

※ Don't Care

"H" level, and that of TC4515BP is selected to "L" level.

When INHIBIT input is set to "H" level, the selection is inhibited regardless of other inputs. In addition, a 4-bit latch function is added to TC4514BP or TC4515BP. If the STROBE input is set to "H" level, this decoder can be applied as a general decoder; however, when the STROBE input is changed from "H" level to "L" level, the output corresponding to binary input at fall time is kept selected. No output changes before STROBE input rise, though binary input changes.

(2) Encoder

TC4532BP is an 8-bit priority encoder which detects "H" level signal of the highest order among eight input signal lines, $D_0 \sim D_7$, and outputs the binary signals of 3 bits. When the input signal is given, the output GS produces "H" level. When ENABLE input is set to "L" level, all the outputs becomes "L" level, and the encode operation is inhibited.

(3) BCD-to-7-Segment decoder

The LED, LC digitron, etc. are largely used for indicating decimal numerical readout. In this case, it is ideal for reading the decimal by human eys that the indication is made by the digital style. Fig. 2-44 shows 7-segment indication style which is the most popular style of indication.

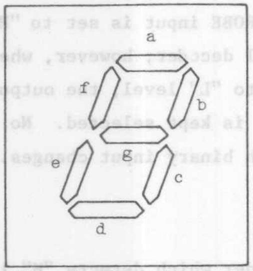


Fig. 2-44 7-Segment Indication Style

In 7-segment indicator, the numerical of 0 to 9 are indicated by lighting or blanking the optical segments of a to g.

For this purpose, the decoder for driving 7 segment from 4-bit BCD input signals is usually used. Further, since the indication is prerequisite for this type decoder, usually the decoder is of the so-called decoder/driver style including the driver of indicator.

With C^2MOS IC, TC4511BP/TC5002BP/TC5022BP are available as the decoders/drivers for LED indicator, and TC4055BP/TC4056BP/TC 4543BP are available for LCD indicator.

For LED drive, LED elements require the constant current of several mA + ~+ several 10mA(DC) for lighting; therefore, the decoder/driver output is of the style capable of current driving.

Concretely speaking, as shown in Fig. 2-46, the configuration is so arranged as to drive the source current of output in the form of adding NPN transistor to CMOS inverter output. Therefore, cathod common type LED display is connected to the output through the resistors for limiting current.

Fig. 2-45 shows the equivalent circuits of TC5002BP/TC5022BP. These decoders/drivers are all provided with the ripple blanking function for facilitating the reading zero suppress at the time of carrying out the multi-digit static driving. And by setting the blanking input to "H" level, all the outputs unconditionally become "OFF", and no display is made.

Fig. 2-46 shows the equivalent circuit of TC4511BP. For TC4511BP, four BCD input lines are provided with latch function. If LE latch-enable input is set to "L" level, the code applied to BCD input is output as it is, but if LE input is set to "H" level, BCD input data at the rise time are latched, and the output indication is fixed until LE is set to "L" level.

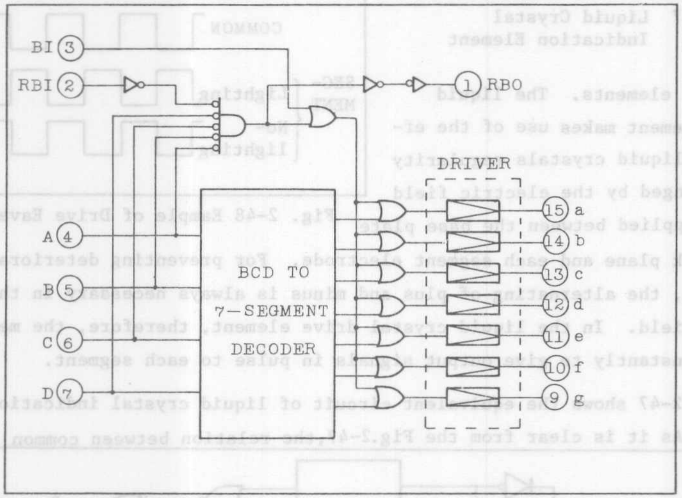


Fig. 2-45 Internal Equivalent Block Diagram

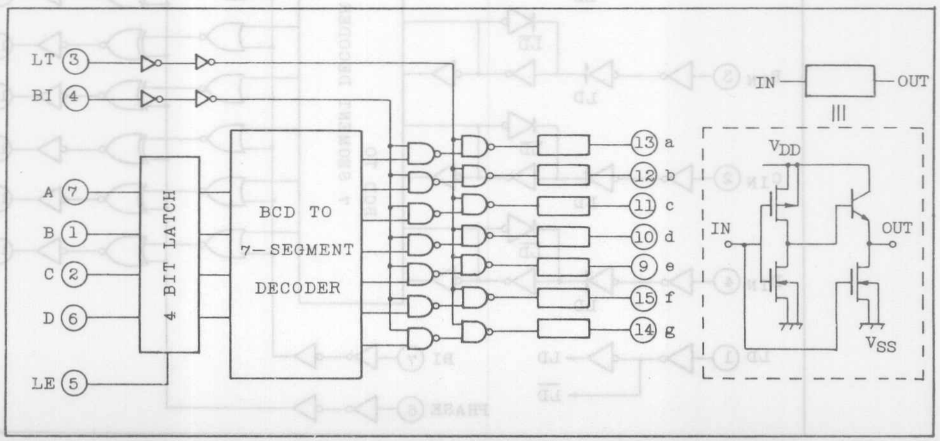


Fig. 2-46 Internal Equivalent Block Diagram

Because of low power consumption performance, recently the liquid crystal element has rapidly been used in larger quantities together with CMOS for electronic calculators, watches, etc. as compared with other indication elements. The liquid crystal element makes use of the effect that liquid crystals regularity being arranged by the electric field which is applied between the base plate called back plane and each segment electrode. For preventing deterioration in element, the alternating of plus and minus is always necessary in this electric field. In the liquid crystal drive element, therefore, the method is used constantly to give output signals in pulse to each segment.

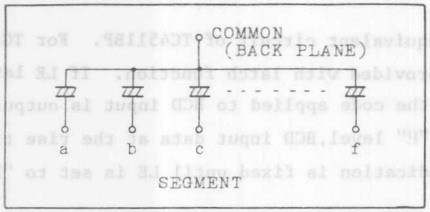


Fig. 2-47 Liquid Crystal Indication Element

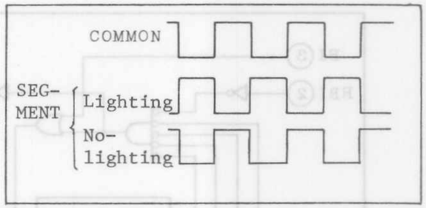


Fig. 2-48 Eample of Drive Eaveform

Fig. 2-47 shows the equivalent circuit of liquid crystal indication element. As it is clear from the Fig.2-47, the relation between common input

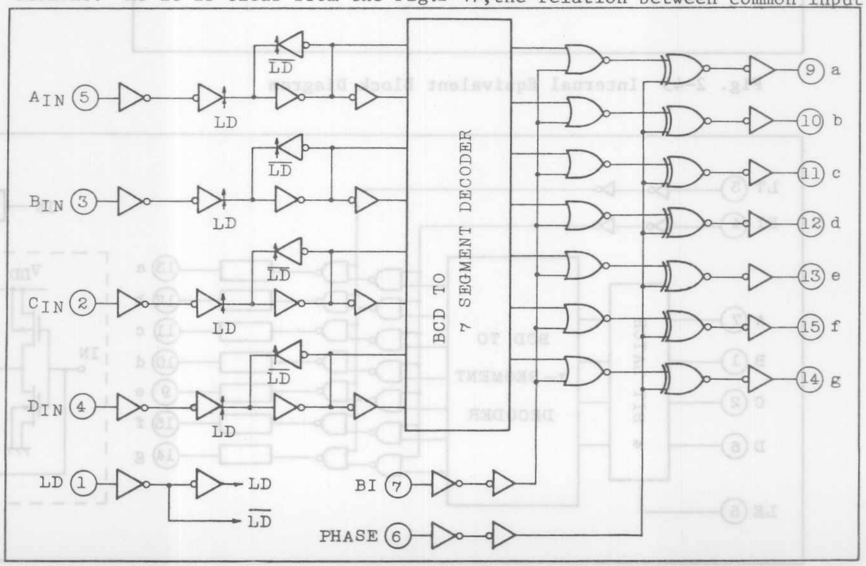


Fig. 2-49 TC4543BP Logical Circuit Diagram

and segment is in the form of being connected to a constant capacity.

Fig. 2-48 shows an example of field effect type static drive waveforms. Lighting segment produces the waveform different in phase by 180° from common pulse, while no-lighting segment produces the same waveform in phase as common pulse.

Fig. 2-49 shows the logic diagram of TC4543BP. TC4543BP is BCD-to-7 segment decoder/LC driver haivng latch function and blanking input. In case the phase input is at "H", each segment output becomes "L" level active; in case the phase input is at "L", each segment output becomes "H" level active.

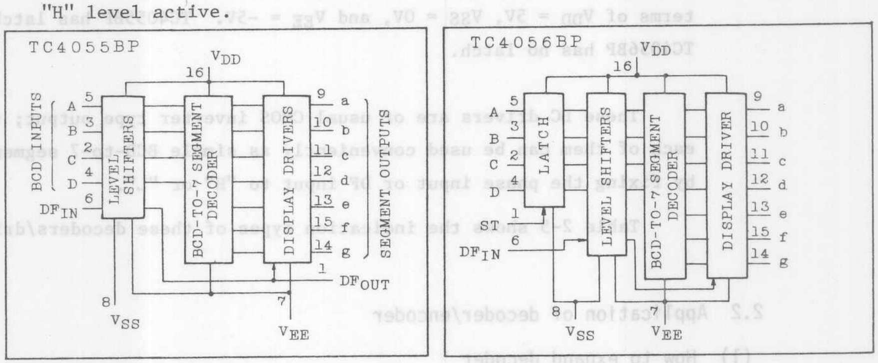
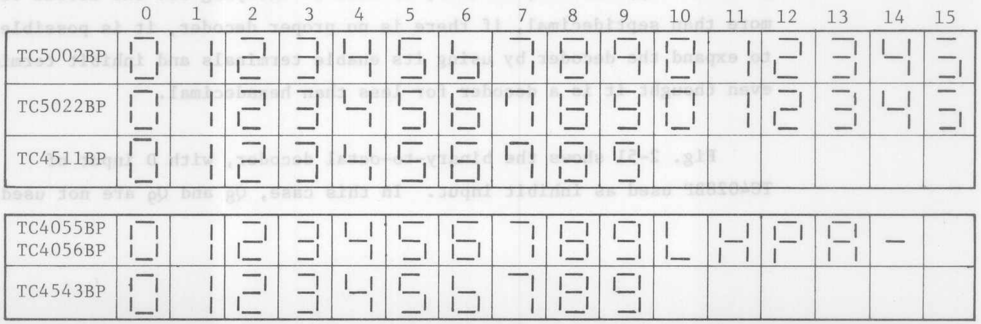


Fig. 2-50 TC4055BP/TC4056BP

Table 2-5 Decoder/Drivers Indication Modes



Therefore, phase signals must be provided in pulse to the back plane and antiphase pulse for phase pulse be applied to each segment to light.

Fig. 2-50 is the block diagrams of TC4055BP/TC4056BP. Since both TC4055BP and TC4056BP have two minus side supply voltages of V_{SS} and V_{EE}, usually they are used as $V_{SS} = V_{EE}$. However, in case the rated voltage of liquid crystal is higher than the voltage of logic current, it is possible to make the logic swing large by using the two lines as $V_{EE} < V_{SS}$. For example, when the rated voltage of liquid crystal is 10V and the voltage of logic circuit is 5V, it is possible to take out the output logic swing of -5V ~ +5V at the input amplitude of 0V ~ 5V in terms of V_{DD} = 5V, V_{SS} = 0V, and V_{EE} = -5V. TC4055BP has latch, while TC4056BP has no latch.

These LC drivers are of usual CMOS inverter type output; therefore, each of them can be used conveniently as simple BCD-to-7 segment decoder by fixing the phase input or DF input to "H" or "L".

Table 2-5 shows the indication types of these decoders/drivers.

2.2 Application of decoder/encoder

(1) How to expand decoder

As explained in the preceding section, the decoders for binary (or BCD) → N (decimal), are available for quadrinary ~ hexadecimal. In the practical application, however, in case of carrying out the decode for more than septidecimal, if there is no proper decoder, it is possible to expand the decoder by using its enable terminals and inhibit terminals even thought it is a decoder for less than hexadecimal.

Fig. 2-51 shows the binary-to-octal decoder, with D input of TC4028BP used as inhibit input. In this case, Q_8 and Q_9 are not used.

Fig. 2-52 shows binary-to-octal decoder using TC4555BP (or TC4556BP). In this case, one inverter is required for substituting the enable input for the highest order binary input.

Fig. 2-53 shows the binary-to-16 line decoder using two devices of TC4028BP base on the same conception as shown in Fig. 2-52. Similarly, by substituting in inhibit inputs of TC4514BP/TC4515BP for most significant bit (MSB), 32-bit decoders can readily be configured. Here the explanation of the relative circuits are omitted.

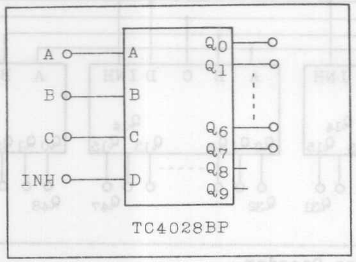


Fig. 2-51 Binary-to-Octal Decoder (1)

Fig. 2-54 shows the binary-to-64 line decoder using four units of TC4514BP.

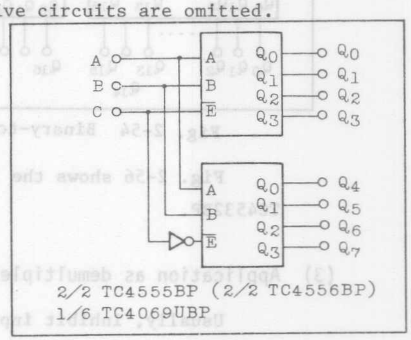


Fig. 2-52 Binary-to-Octal Decoder (2)

(2) How to expand encoder

The encoder as MSI is TC4532BP only. As TC4532BP is provided with mode input and output function such as enable input and output, GS output, etc., this encoder can easily expand the input and output lines.

Fig. 2-55 shows the decimal-to-BCD priority gated decoder. It is advantageous for conversion from ten keys into BCD information.

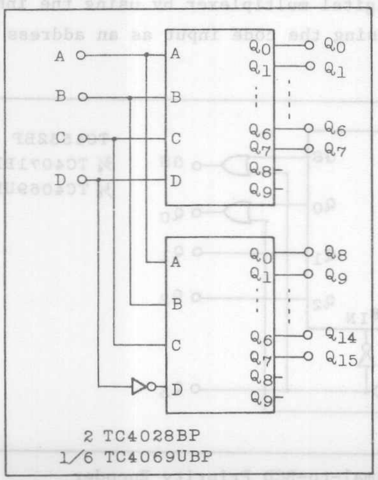


Fig.2-53 Binary-to-16 Line Decoder

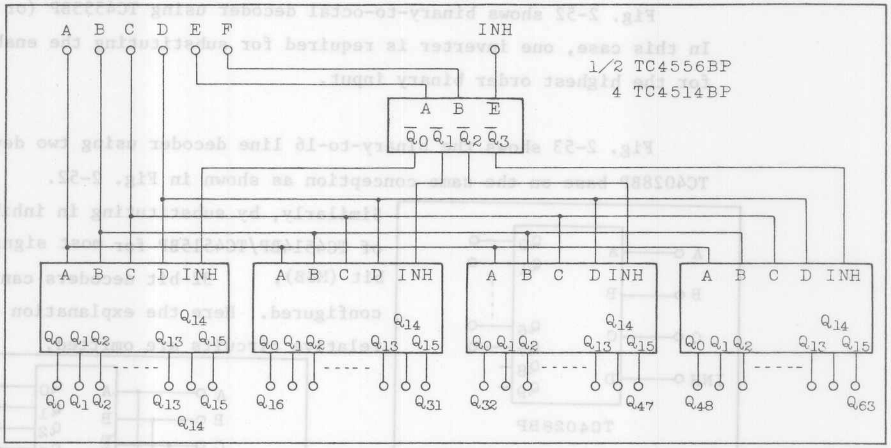


Fig. 2-54 Binary-to-64 Line Decoder

Fig. 2-56 shows the 16-bit priority encoder connecting two units of TC4532BP.

(3) Application as demultiplexer

Usually, inhibit input and enable input are provided with CMOS decoder. In general, these inputs are used for inhibiting decode. However, the decoder can be used as the digital multiplexer by using the inhibit (enable) as a data input by using the code input as an address input.

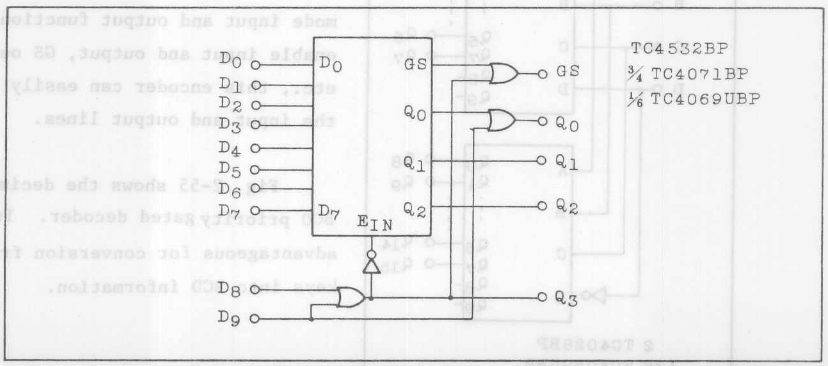


Fig. 2-55 Decimal-to-BCD Priority Encoder

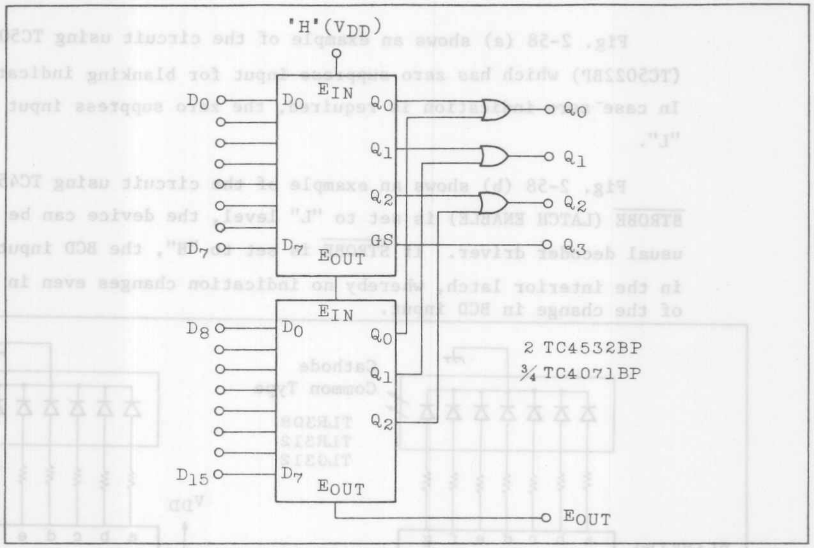
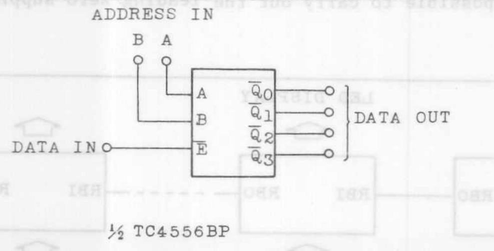


Fig. 2-56 16-Bit Priority Encoder

Demultiplexer is the circuit for taking out one input line signal as an optional input in "N" units of output lines according to the address input. This can be considerd as the substitution of a rotary switch. Fig. 2-57 shows the 4-channel demultiplexer using TC4556BP. The same circuit can be configurated by using TC4515BP or TC4028BP.

(4) Static LED display drive circuit

Fig. 2-58 shows one digit LED drive circuit.

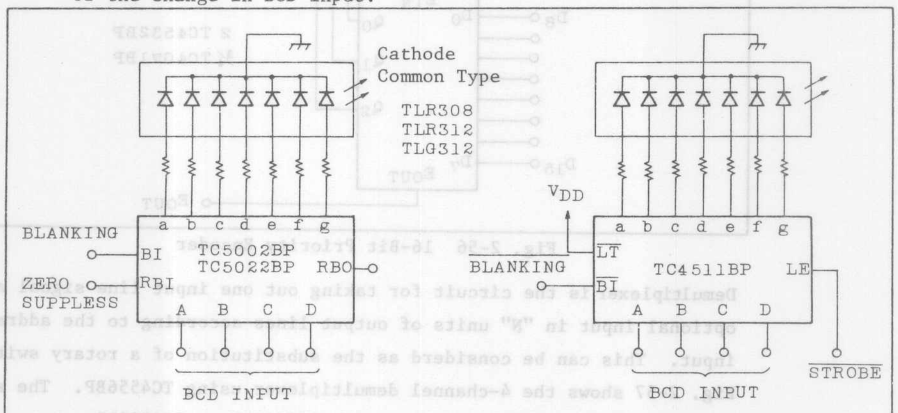


A	B	$\overline{E}$	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$
L	L	L	L	H	H	H
L	L	H	H	H	H	H
H	L	L	H	L	H	H
H	L	H	H	H	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	H
H	H	L	H	H	H	L
H	H	H	H	H	H	H

Fig. 2-57 4-Channel Demultiplexer

Fig. 2-58 (a) shows an example of the circuit using TC5002BP (TC5022BP) which has zero suppress input for blanking indication. In case zero indication is required, the zero suppress input is set to "L".

Fig. 2-58 (b) shows an example of the circuit using TC4511BP. If $\overline{\text{STROBE}}$ (LATCH ENABLE) is set to "L" level, the device can be used as a usual decoder driver. If $\overline{\text{STROBE}}$ is set to "H", the BCD input is held in the interior latch, whereby no indication changes even in the case of the change in BCD input.



(a) With zero suppress function (b) With latch

Fig. 2-58 One Digit LED Drive Circuit

In case of driving "N" digits, fundamentally N units of the circuit shown in Fig.2-58 have only to be used. In the case of TC5002BP (TC5022BP), however, it is possible to carry out the leading zero suppress by using RBI and RBO.

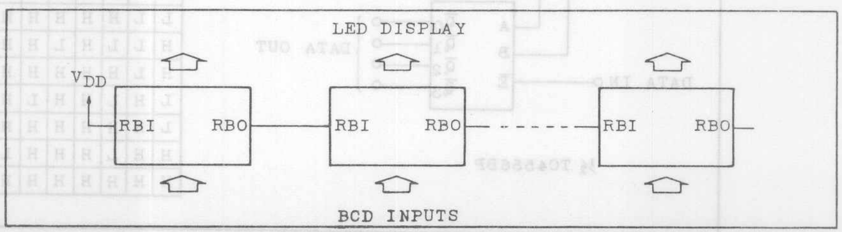


Fig.2-59 N-Digits Leading Zero Suppress Drive Circuit by TC5002BP

When LED drive is carried out by using TC5002BP or TC4511BP, the current limit resistance "R" is decided by the drawing shown in Fig. 2-60.

In the figure, in case T_{DD}=5V, V_{OH} and I_{OH} curves of TC5002BP are provided by a and a' (a being 25°C standard characteristic and a' being 85°C minimum characteristic). For example, therefore, if I_{OH} is flown by 10 mA, Q_5 on a' curve becomes the operating point. By drawing perpendiculary a line from Q_5 to axis of abscissa, the intersection point becomes the output voltage V_{OH5}.

Therefore, the remaining voltage (V_{OH5}-2V) after deducting the forward voltage drop (approx. 2V) of GaP type LED from V_{OH5} is applied to both ends of "R", whereby, the triangle given by

$$\underset{(\text{at } V_{DD}=5V)}{R} = \frac{V_{OH5} - 2}{10 \times 10^{-3}}$$

and comprising V_F - Q_5 - V_{OH5} being in resemblance with the triangle comprising V_F - i_5 - 5V,

$$R = \frac{5V - V_F}{i_5} = \frac{3}{18} \times 10^3 \doteqdot 170\ [\Omega]$$

In the case of V_{DD}=10V,15V, the resistances are obtained in the same manner as quoted above.

In general, the following formula is established:

$$R = \frac{V_{PP} - V_P}{i}$$

Note) i point shall be obtained by drawing figures.

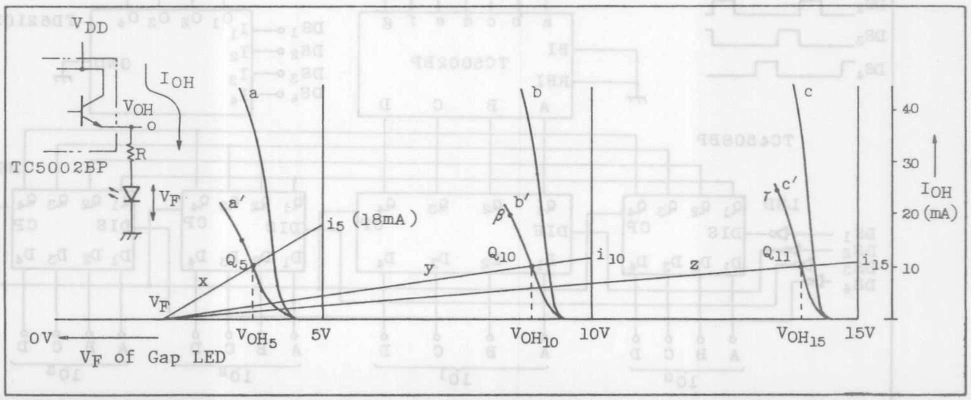


Fig. 2-60 How to Obtain Operating Point of Static LED Drive Cricuit

(5) Dynamic LED display drive circuit

The dynamic LED display drive circuit is a circuit for using the decoder driver by means of time sharing in the case of lighting multi-digit LED. Fig.2-61 shows the 4-digit LED drive circuit using TC5002BP. In the same figure, this circuit is configurated by the use of the latch TC4508BP with three state output, whereby making 4-digit BCD input multiplex, making the enable signals of multiplexer $DS_1 \sim DS_4$ correspond to the base input of digit selecting driver TD62103P (Darlington transistor array) at the ratio of 1 to 1.

In the case of practical applications, if code input is fed in the state of static input as shown in the same figure, the merits of dynamic drive are reduced by reason of having to add multiplexer, driver, etc. to the circuit. However, the practical application of circuit becomes a very effective driving method.

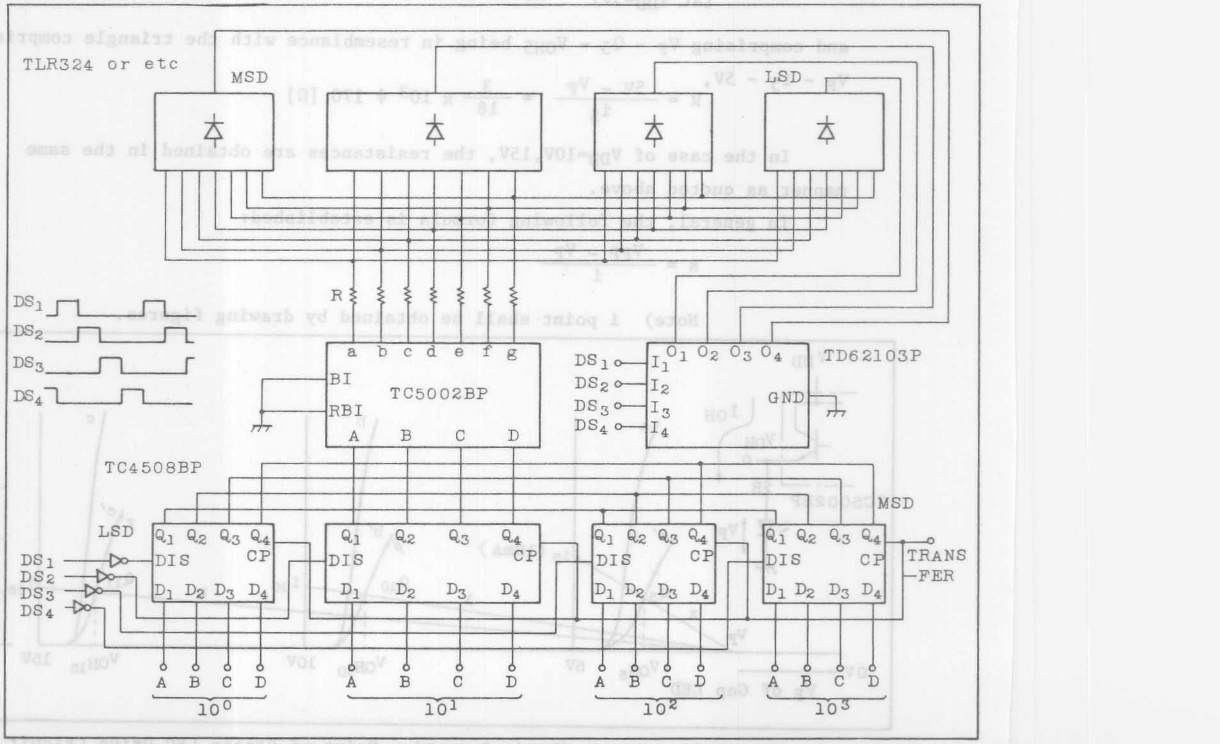


Fig. 2-61 4 - Digit LED Drive Circuit

It is very useful for the LSI output to be sent in the state of dynamic output or data to sent to bus line by using time sharing,so that those peripheral CMOS IC such as multiplexer are omited.

(6) Static liquid crystal drive circuit

Fig. 2-62 shows the single digit liquid crystal drive circuit using TC4056BP/TC4543BP. The same square wave is given to common terminal of liquid crystal and DF (or PH) input of driver. Fig. 2-63 shows the examples of square wave generating circuit.

Fig. 2-63 (a) shows an example of the oscillator using the variable resistor for causing the duty cycle to 1/2, while Fig. 2-63 (b) shows an example of the oscillator using flip-flop. Such an oscillator is, of course, not required if there is approx.32Hz clock existing in the system.

In the practical use, most liquid crystal indicators are of multi-digit, so that the displaying drivers are used in parallel according to the number of digits. In this case, the capacitance of common terminal of liquid crystal reaches approx. 1000pF ~ 5000pF; therefore, the current driver is required to refrain from directly driving of LCD by C^2MOS output.

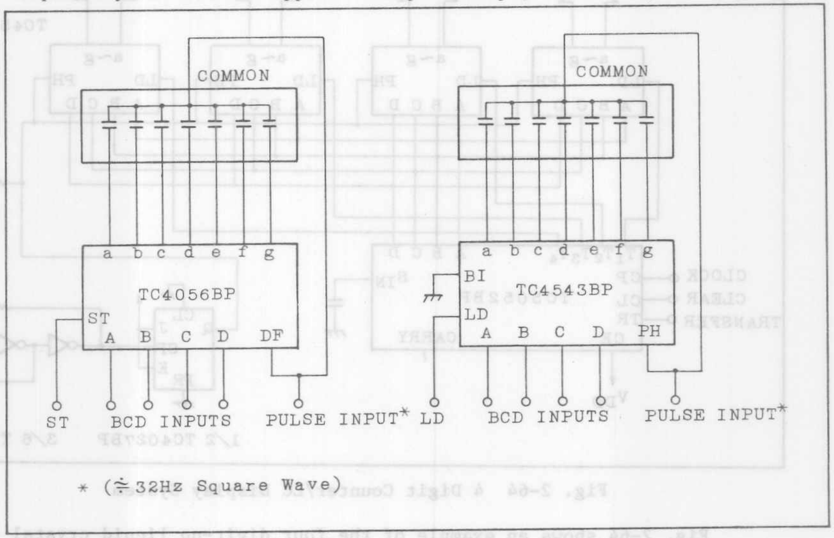


Fig. 2-62 1-Digit LCD Drive Circuit

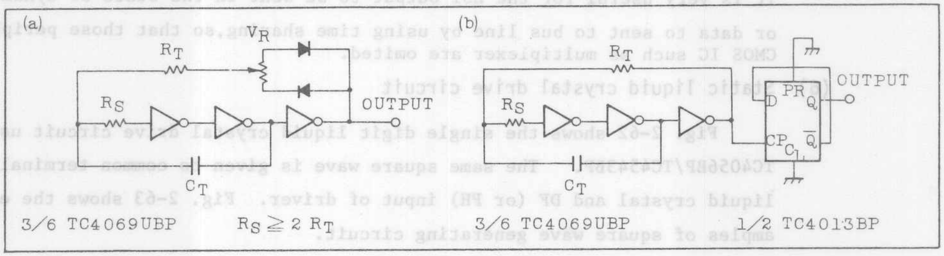


Fig. 2-63 Square Wave Oscillator

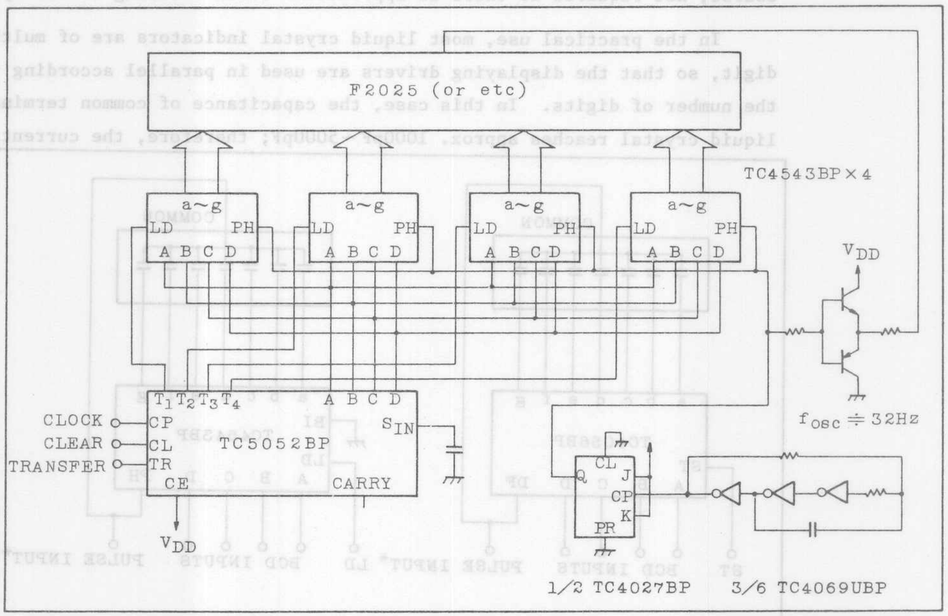


Fig. 2-64 4 Digit Counter/LC Display System

Fig. 2-64 shows an example of the four digit-up liquid crystal display counter using TC5052BP and TC4543BP, while Fig. 2-65 shows an example of the four digit up-and-down liquid crystal display counter using TC5010P and TC5064BP.

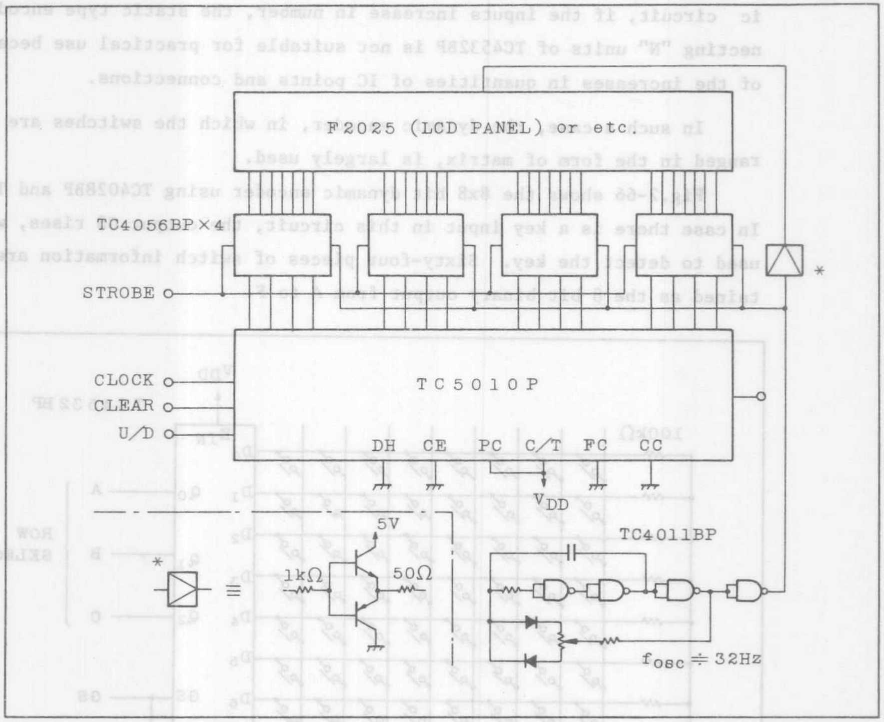


Fig. 2-65 4 Digit Up/Down Counter/LC Display System

(7) Dynamic encoder

In case of putting the key information as the input into the electronic circuit, if the inputs increase in number, the static type encoder connecting "N" units of TC4532BP is not suitable for practical use because of the increases in quantities of IC points and connections.

In such a case, the dynamic encoder, in which the switches are arranged in the form of matrix, is largely used.

Fig.2-66 shows the 8x8 bit dynamic encoder using TC4028BP and TC4532BP. In case there is a key input in this circuit, the output GS rises, which is used to detect the key. Sixty-four pieces of switch information are obtained as the 8 bit binary output from A to F.

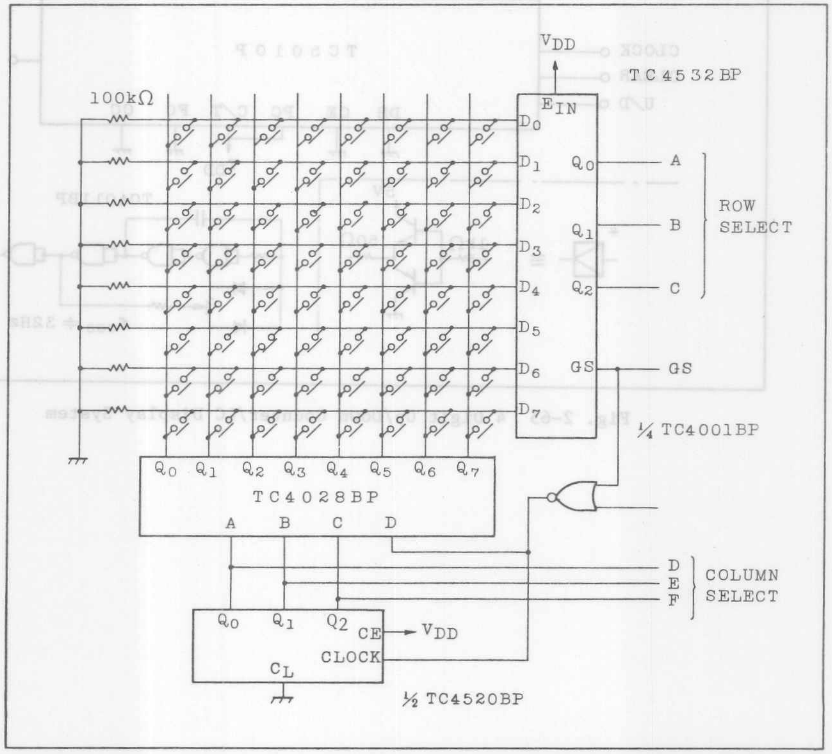


Fig. 2-66 8 x 8 C^2MOS Dynamic Encoder

3. Multiplexer/Demultiplexer

The multiplexer is the data selector selecting the information of one arbitrary input line out of "N" number of input lines according to the address input. Demultiplexer has the function of distributing the information of one input line out of arbitrary outputs of "N" number of outputs according to the address input. These functions can be regarded as those of mechanical rotary switch manufactured electronically.

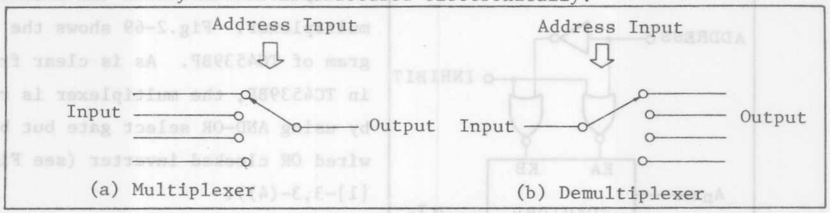


Fig. 2-67 Multiplexer and Demultiplexer

Fig.2-67 illustrates the functions of multiplexer and demultiplexer for easy understanding. In C^2MOS IC there are digital level multiplexer structuring logic functions and analog level multiplexer applying the analog switch. As mentioned in the preceding Section, there are no exclusive products for digital level multiplexer, which can be accomplished with the application of decoder. The analog level demultiplexer is equivalent to analog multiplexer, because the analog switch itself is bidirectional.

3.1 Approach to multiplexer/demultiplexer

Table 2-6 is the list of C^2MOS multiplexers and demultiplexers.

Table 2-6 List of C^2MOS Multiplexers and demultiplexers

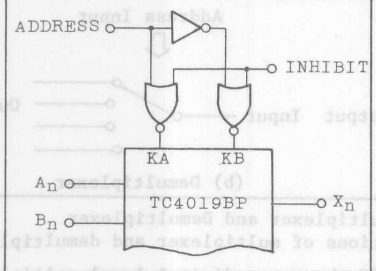
No.of Channels	Digital		Analog
	Multiplexer	Demultiplexer	Multiplexer/Demultiplexer
2 channels	TC4019BP	—	TC4053BP
4 channels	TC4539BP	(TC4555BP) (TC4556BP)	TC4052BP
8 channels	TC4512BP	(TC4028BP)	TC4051BP
16 channels	TC5023BP	(TC4514BP) (TC4515BP)	—

(1) Digital multiplexer

As is clear from the Table, the digital multiplexers are widely available ranging from 2 channels to 16 channels.

As shown in Fig. 2-1 in [2]-1, 1-(3), TC4019BP is a multiplexer with 2 channels circuits. As shown in Fig.2-68, usually the 2-channel multiplexer selects A_n or B_n input by giving inversion signals to KA input and KB input. TC4539BP is the 2-circuit 4-channel multiplexer. Fig.2-69 shows the logic diagram of TC4539BP. As is clear from the figure, in TC4539BP, the multiplexer is realized not by using AND-OR select gate but by using the wired OR clocked inverter (see Fig.1-11 in [1]-3,3-(4)).

Fig. 2-70 shows the examples of circuits under both systems. In this figure, (a) is just the same in operation as (b).



INPUTS				OUTPUT
Add	INH	A_n	B_n	X_n
※	H	※	※	L
H	L	※	H	H
H	L	※	L	L
L	L	H	※	H
L	L	L	※	L

※ Don't Care

Fig.2-68 2-Channel Multiplexer

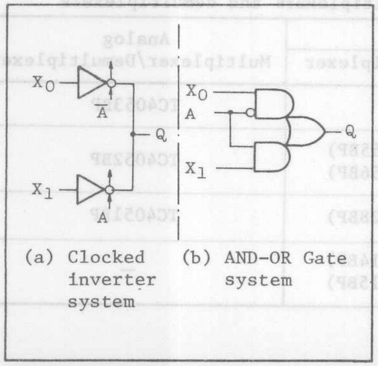


Fig. 2-70 Multiplexer System

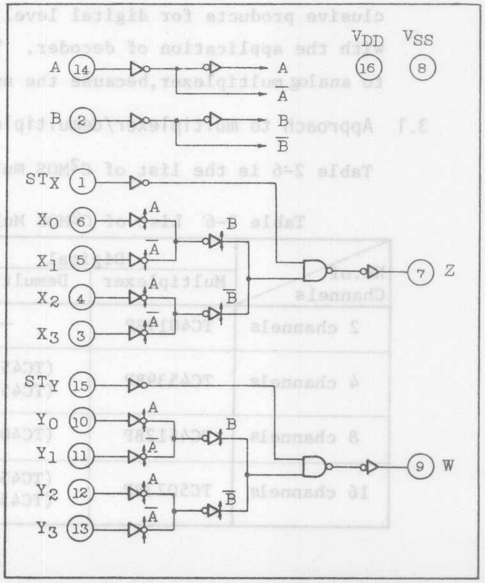


Fig. 2-69 4-Channel Multiplexer

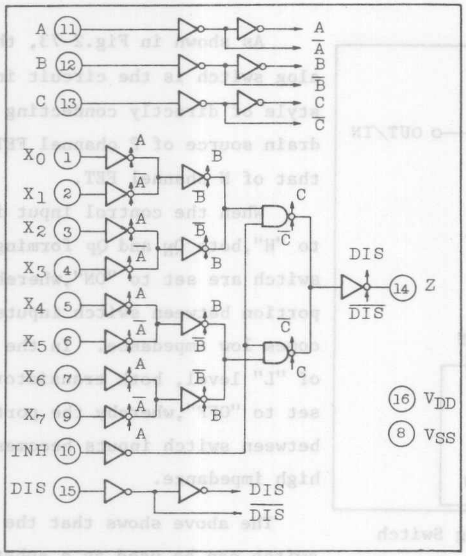


Fig. 2-71 TC4512BP
8-channel Multiplexer

Fig.2-71 shows the 8-channel multiplexer TC4512BP. Being provided with DISABLE input making the output high impedance, TC4512BP is convenient to wired OR, etc.

Fig.2-72 shows the 16-channel multiplexer TC5023BP further increasing the inputs in number.

Unlike TC4539BP and TC4512BP, TC5023BP can obtain the output in the form of inversion. And TC5023BP agrees in its operation and pin connection with TTL74150/54150.

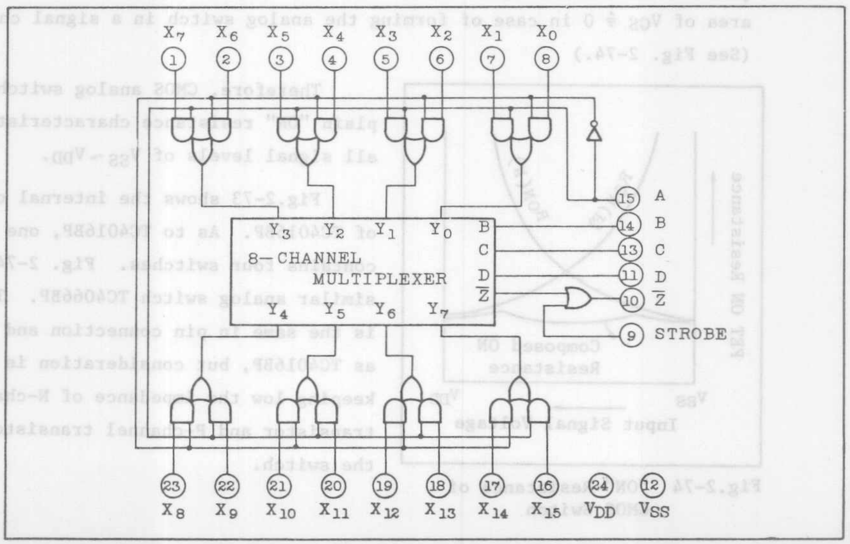


Fig. 2-72 TC5023BP 16-Channel Multiplexer

(2) Analog switch

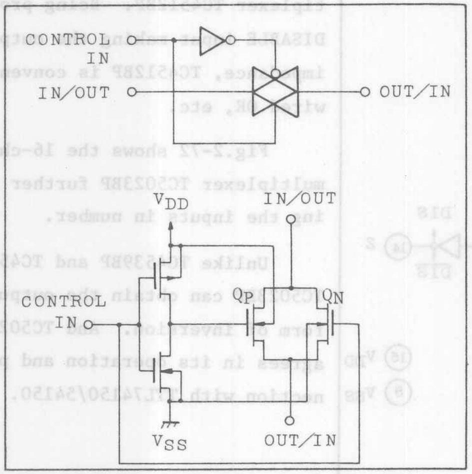


Fig. 2-73 TC4016BP Analog Switch

As shown in Fig.2-73, the analog switch is the circuit in the style of directly connecting the drain source of P channel FET to that of N channel FET.

When the control input is set to "H",both Q_N and Q_P forming the switch are set to "ON",whereby the portion between switch inputs becomes low impedance. In the case of "L" level, both transistors are set to "OFF",whereby the portion between switch inputs becomes very high impedance.

The above shows that the analog switch can be used as a substitute for relay. The reason for using both P-channel and N-channel is to compensate the sudden change of ON resistance due to the cutoff of FET in the area of $V_{GS} \fallingdotseq 0$ in case of forming the analog switch in a signal channel. (See Fig. 2-74.)

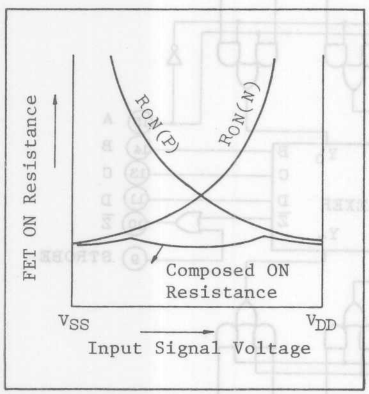


Fig.2-74 "ON" Resistance of CMOS Switch

Therefore, CMOS analog switch shows plain "ON" resistance characteristics on all signal levels of $V_{SS} \sim V_{DD}$.

Fig.2-73 shows the internal circuit of TC4016BP. As to TC4016BP, one package contains four switches. Fig. 2-74 shows similar analog switch TC4066BP. TC4066BP is the same in pin connection and working as TC4016BP, but consideration is given to keeping low the impedance of N-channel transistor and P-channel transistor forming the switch.

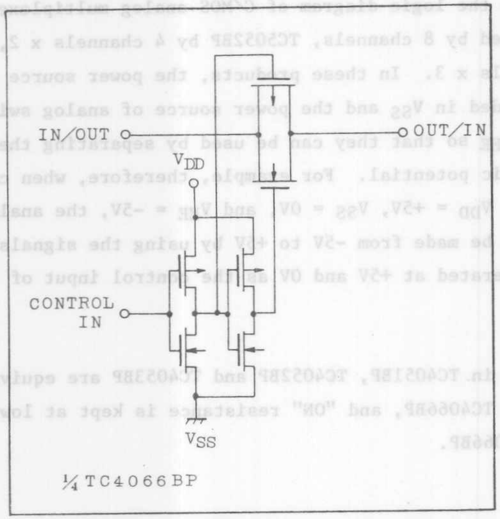


Fig. 2-75 TC4066BP Equivalent Circuit

Therefore, as compared with TC 4016BP, TC4066BP is plain in ON resistance characteristics and small in distortion rate at the time of transmitting signals.

These TC4016BP and TC4066BP can be used not only as the switch for degital signals but also as the switch for analog signals; therefore, they can be used for switching and mixing audio signals and as the input switching signal for A/D converter.

However, in comparison with the mechanical contact, TC4016BP/TC4066BP have the merits, such as

a) Rapid in response speed,

b) Small in power consumption,

c) Low in price,

d) High in actual installation density,

but have the demerits, such as

e) Limit in signal levels ($V_{SS} \sim V_{DD}$),

f) Have ON resistance (Small in allowable current),

g) Have stroke.

Therefore, full consideration should be given to these demerits at the time of designing.

(3) Analog multiplexer/demultiplexer

By using several units of analog switch shown in (2) and connecting in common the one-side inputs, analog multiplexer/demultiplexer can be configurated. Each switch is usually selected with decoder and others bult in.

Fig. 2-76 shows the logic diagram of C^2MOS analog multiplexer. TC5051BP is structured by 8 channels, TC5052BP by 4 channels x 2, and TC5053BP by 2 channels x 3. In these products, the power source of control side is divided in V_{SS} and the power source of analog switch side is divided in V_{EE} so that they can be used by separating the power source of low electric potential. For example, therefore, when connections are made as V_{DD} = +5V, V_{SS} = 0V, and V_{EE} = -5V, the analog signal multiplex can be made from -5V to +5V by using the signals of the logic circuit operated at +5V and 0V as the control input of analog multiplexer.

And each switch in TC4051BP, TC4052BP and TC4053BP are equivalent in circuit system to TC4066BP, and "ON" resistance is kept at low value close to that of TC4066BP.

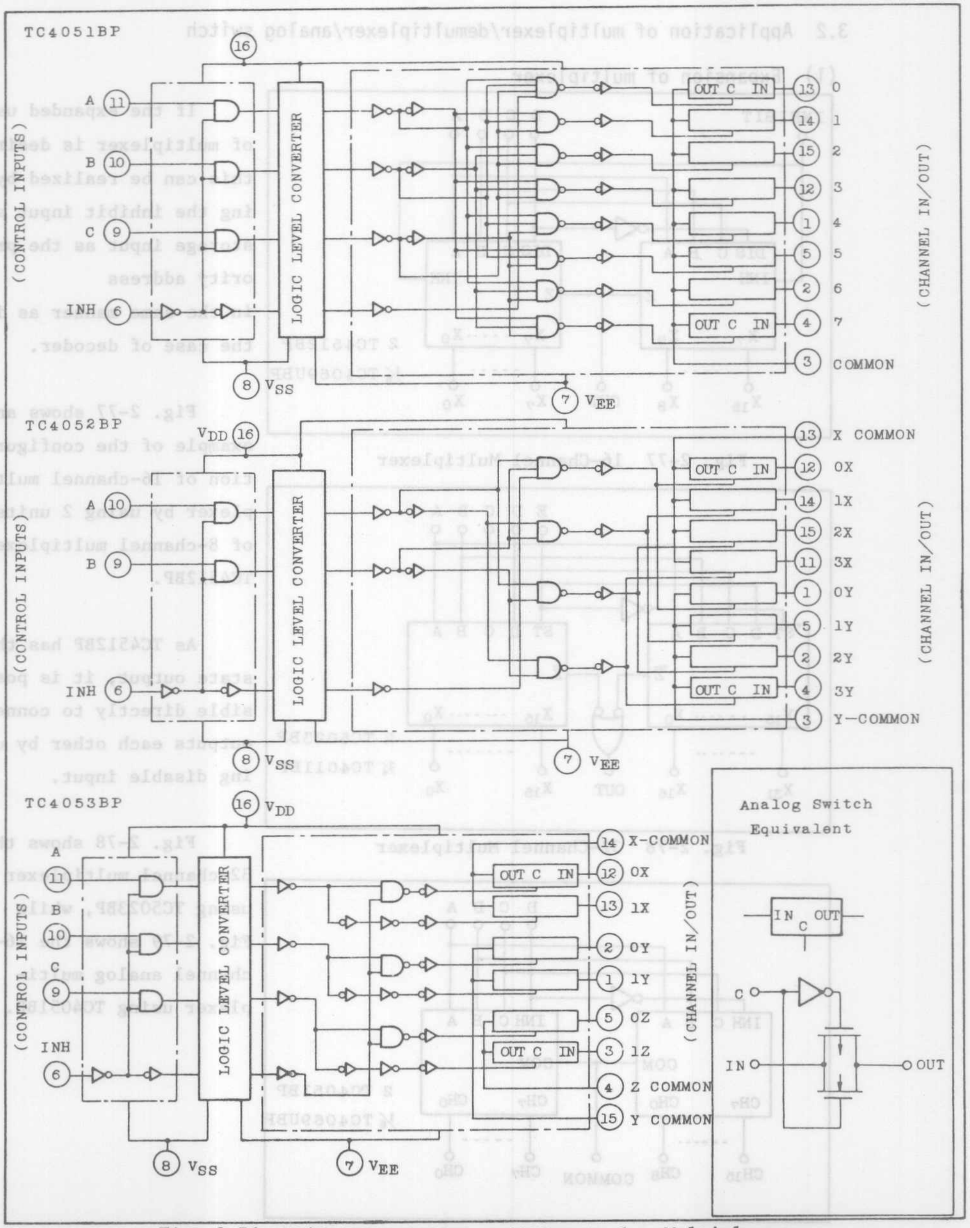


Fig. 2-76 TC4051BP,TC4052BP,TC4053BP Analog Multiplexer

3.2 Application of multiplexer/demultiplexer/analog switch

(1) Expansion of multiplexer

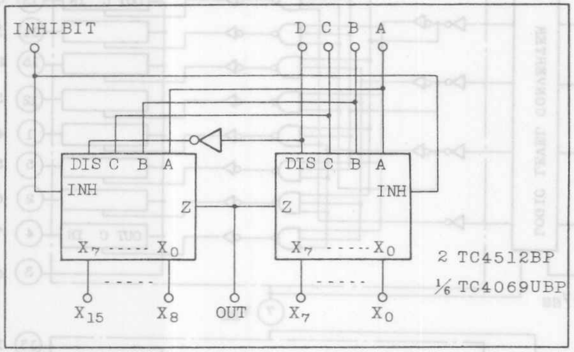


Fig. 2-77 16-Channel Multiplexer

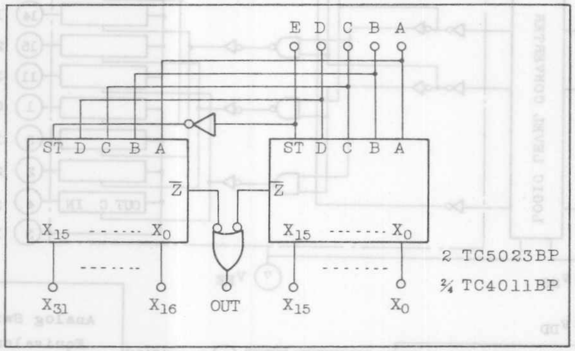


Fig. 2-78 32-Channel Multiplexer

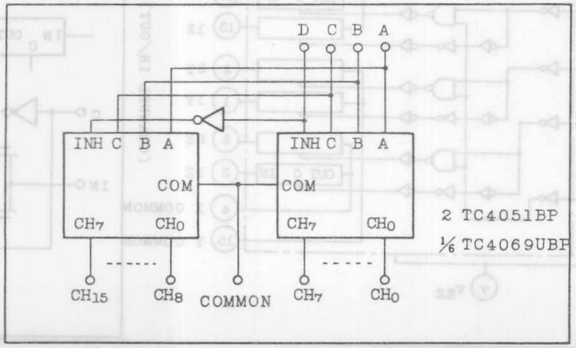


Fig. 2-79 16-Channel Multiplexer

If the expanded use of multiplexer is desired, this can be realized by using the inhibit input and storage input as the priority address in the same manner as in the case of decoder.

Fig. 2-77 shows an example of the configuration of 16-channel multiplexer by using 2 units of 8-channel multiplexer TC4512BP.

As TC4512BP has three-state output, it is possible directly to connect outputs each other by using disable input.

Fig. 2-78 shows the 32-channel multiplexer using TC5023BP, while Fig. 2-79 shows the 16-channel analog multiplexer using TC4051BP.

(2) Substitution to combination logical circuit

In addition to the series conversion of data, the multiplexer can be regarded as the logical circuit of multivariable-one-output. Let us consider the 4-channel multiplexer shwon in Fig. 2-80.

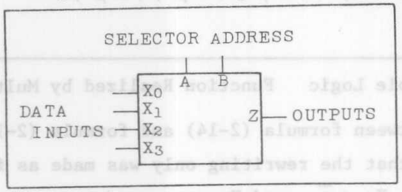


Fig.2-80 4-Channel Multiplexer

The logical formula of this multiplexer is expressed by

$$Z=X_0\cdot\overline{A}\cdot\overline{B} + X_1\cdot A\cdot\overline{B} + X_2\cdot\overline{A}\cdot B + X_3\cdot A\cdot B \quad \text{......} \ (2\text{-}14)$$

Namely, by using address inputs of A and B and data input of X, it is possible to take out the data given to input as the logic output at 2.

For example, let us consider the circuit having the truth value shown in Table 2-7. The Table can be expressed by the following logical formula;

Table 2-7

γ	β	α	F
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

$$F = \alpha\cdot\overline{\beta}\cdot\overline{\gamma} + \overline{\alpha}\cdot\beta\cdot\overline{\gamma} + \overline{\alpha}\cdot\overline{\beta}\cdot\gamma + \alpha\cdot\beta\cdot\gamma \quad \text{.....} \ (2\text{-}15)$$

Table 2-7 is rewritten to Fig. 2-81 by using Karnaugh diagram. (In the Fig., "H" → 1, "L" → Blank.)

By separating the logic variable α, Fig. 2-81 is divided into two Karnaugh diagrams as shown in Fig. 2-82.

Returning to Fig.2-80, by making the address inputs of A and B corresponded to β and γ in Karnaugh diagram of Fig. 2-82, it follows that the data inputs $X_0 \sim X_3$ correspond to each square as shown in Fig. 2-83.

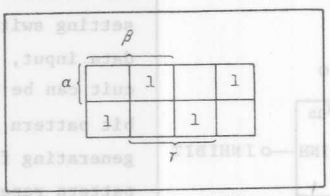


Fig. 2-81 Karnaugh Diagram

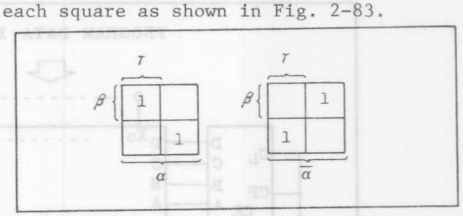


Fig.2-82 Division of Karnaugh Diagram

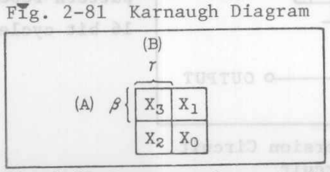


Fig.2-83 Correspondence to Muptiplexer

By the combination of Fig.2-82 and Fig. 2-83, $X_0=\alpha$, $X_1=\overline{\alpha}$, $X_2=\overline{\alpha}$, and $X_3=\alpha$ are led out, and it is found that the multiplxer has only to be connected as shown in Fig. 2-84.

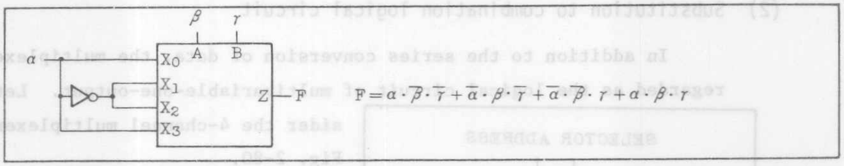


Fig. 2-84 Example of 3-Variable Logic Function Realized by Multiplexer

The comparison is made between formula (2-14) and formula (2-15).

In both formulas, it is found that the rewriting only was made as follows:

$A \to \beta$, $B \to \gamma$, $X_0 \to \alpha$, $X_1 \to \overline{\alpha}$, $X_2 \to \overline{\alpha}$, and $X_3 \to \alpha$

In this example, the explanation was made in due order for easy understanding. In general, however, the logic function of three variable is realized by using the above-mentioned procedures.

In the case of four variables, the 8-channel multiplexer provided with three address inputs is used. In the case of five variables, the 16-channel multiplexer is used. Namely, if the binary addresses of multiplexer are four in number, it is possible to realize the logic function up to 4 + 1 variables. The example was quoted from three-input exclusive logic sum. In the case of other circuits, however, multiplex input may be fixed to "H" or "L".

(3) Parallel series conversion circuit

For selecting one output out of "N" inputs, by scanning in due order the address inputs by using a counter, the multiplexer can send in due order the parallel inputs as the outputs of series data.

Fig.2-85 shows the parallel series conversion circuit using TC5023BP and TC4520BP. By setting switably the data input, this circuit can be used as the 16-bit pattern generator generating free serial pattern repeated in 16 bit cycles.

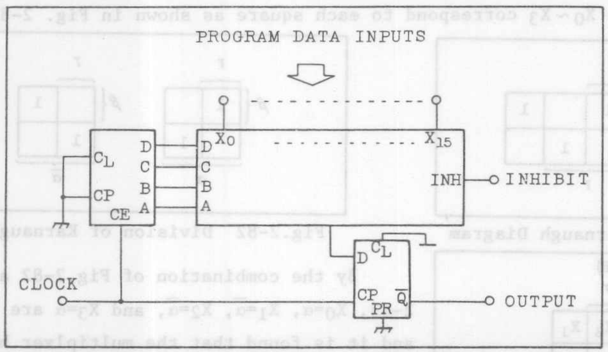


Fig.2-85 16-bit Parallel Series Conversion Circuit
16-bit pattern Generator Circuit

(4) Bidirectional data selector

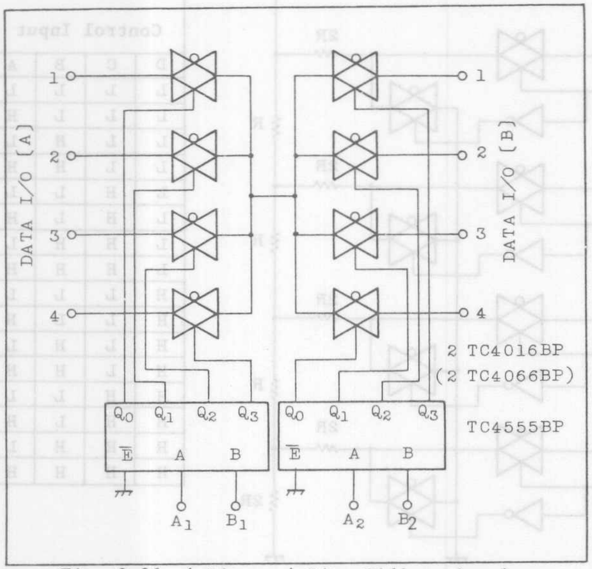


Fig. 2-86 4 Bits - 4 Bits Bidirectional Data Selector

Analog switches are capable of switching on and off linear signals,and various switch alleys can be composed by combining these switches.

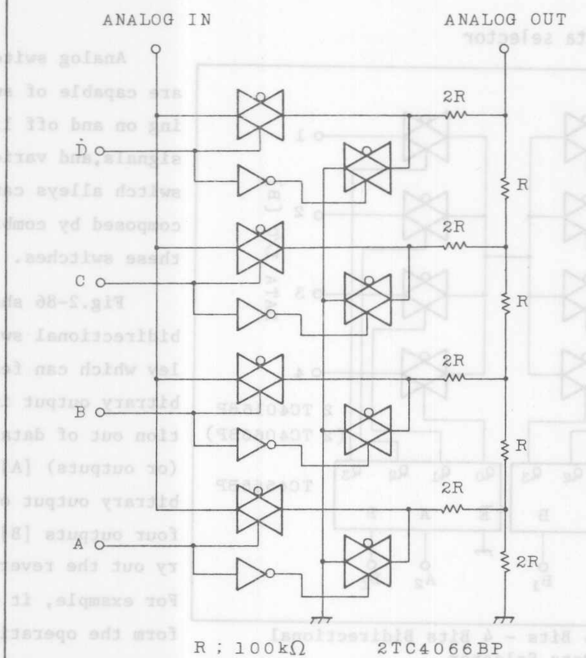
Fig.2-86 shows the bidirectional switch alley which can feed an arbitrary output information out of data inputs (or outputs) [A] to an arbitrary output out of four outputs [B] (or carry out the reverse function.) For example, it can perform the operation like telephone exchange.

(5) Programable attenuator

Fig. 2-87 shows the programable signal attenuator using TC4066BP. TC4066BP consists of four-circuit analog data selector, and one input is connected to the analog input and the other input is connected to GND. When RADA network of R-2R is composed, the output makes it possible to automatically divide voltage for each 1/16 from 0 to 15/16 according to the control addresses of A to D.

(6) Data transmission circuit

In the case of carrying out data transmission, if the distance between transmission side and reception side is long, it is rather advantageous to transmit data under time sharing system than to prepare the transmission lines equal in number to the signal lines.



Control Input				Potential Ratio
D	C	B	A	A_0/A_i
L	L	L	L	0
L	L	L	H	1/16
L	L	H	L	1/8
L	L	H	H	3/16
L	H	L	L	1/4
L	H	L	H	5/16
L	H	H	L	3/8
L	H	H	H	7/16
H	L	L	L	1/2
H	L	L	H	9/16
H	L	H	L	5/8
H	L	H	H	11/16
H	H	L	L	3/4
H	H	L	H	13/16
H	H	H	L	7/8
H	H	H	H	15/16

Fig. 2-87 Programmable Signal Attenuator

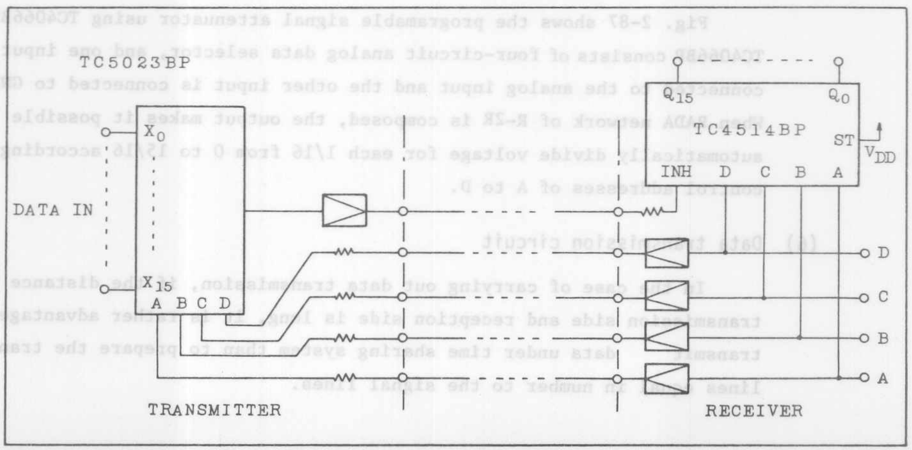


Fig. 2-88 16-Bit Data Transmitting System

Usually, the data are transmitted serially according to the clock by using the shift register, etc. In this case, however, the extra control is required for synchronization between transmission side and reception side.

Fig. 2-88 shows the most fundamental data transmission system, for which no clock is required. The data inputs corresponding to the address inputs of A to D are obtained on the data outputs corresponding at the same time.

(7) Sine wave generating circuit

Fig. 2-89 shows the sine wave generating circuit capable of digitally generating sine waves. In many cases the generation of sine waves by logic circuit is made by using D/A converter, etc. Here, however, the generation of sine waves is accomplished by using C^2MOS up-and-down counter TC4510BP and analog multiplexer TC4051BP.

By using TC4510BP, TC4013BP and some gates, it is possible to accomplish the counter preparing the multiplexer control signals. This counter reciprocates automatically between up-mode and down-mode, Namely, the count condition is as given below:

$$\underbrace{4 \to 5 \to 6 \to 7 \to 8}_{\text{UP}} \to \underbrace{7 \to 6 \;\ldots\ldots \to 2 \to 1 \to 0}_{\text{DOWN}} \to \underbrace{1 \to 2 \;\ldots\ldots}_{\text{UP}}$$

By adding the BCD data in due order to the 9-channel multiplexer composed by TC4051BP and TC4066BP, the voltage in the range of $V_1 \sim V_2$ can be obtained in order as an output.

The level which was obtained by the quantization of sine waves through resistance potential dividing is given to the multiplexer input, in advance. In this case, however, V_1 and V_2 are required to be within the supply voltage range of multiplexer. This circuit is sufficiently suitable for practical use by means of inserting filter in the output to reduce the distorsion rate of high frequency and to make impedance conversion with voltage follower. By dividing the clock frequency into 1/N, the output frequency becomes 1/N, resulting in the possibility of using this circuit as a simple oscillator.

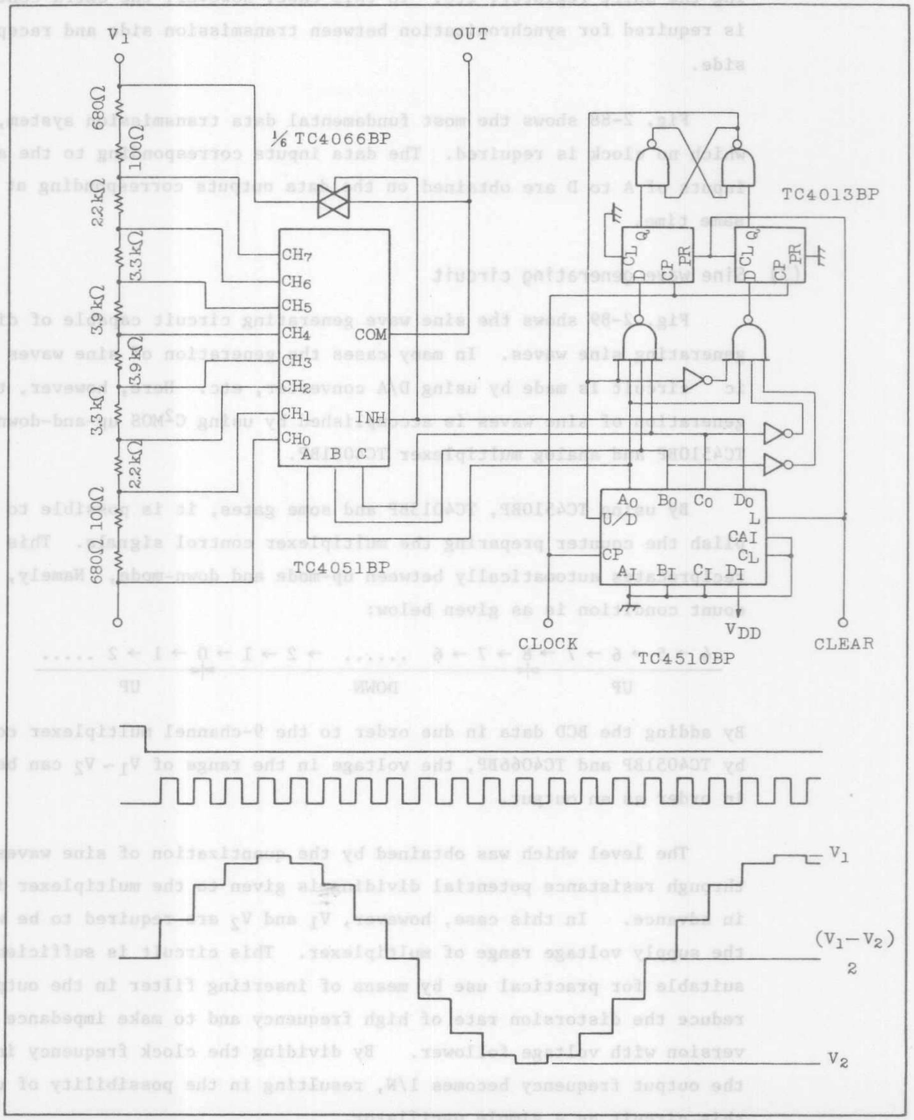


Fig. 2-89 Sine Wave Generating Circuit

4. Latch/flip-flop

Generally, unlike such circuits of gates, decoders, multiplexers, etc. (these are combined into logic circuit) as mentioned before, latch/flip-flop and their applied products of counter and shift resister are of the circuit having memory elements in the interior. In the combined logic circuit, if the input logic function at arbitrary time is given, all the outputs are decided by input logic condition only. In the sequential logic circuit, however, the output is decided by the input information at arbitrary time and by the internal memory information. In other words, the output is decided by the

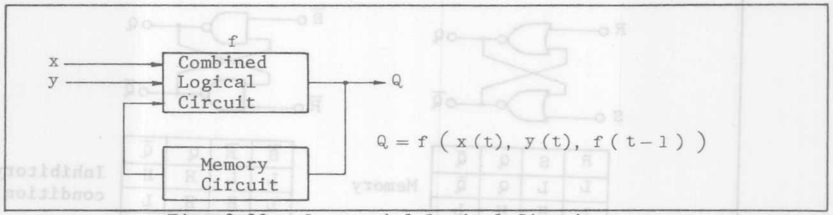


Fig. 2-90 Sequential Logical Circuit

input funciton at arbitrary time and the input function at the bit time just before the arbitrary time.

Fig 2-90 shows the conceptional diagram of the sequential logic circuit. Now, explanation is made on the flip-flop, which is the base of memory circuit.

4.1 Latch/flip-flop circuits

In a broad sense, a latch circuit is a kind of flip-flop. The flip-flop circuit is another name of bistable multivibrator (the circuit having two stable states). In the binary logic circuits including C^2MOS IC, the above-mentioned two stable states correspond to "H" (Positive logic 1) and "L" (Positive logic 0).

(1) Storage cell

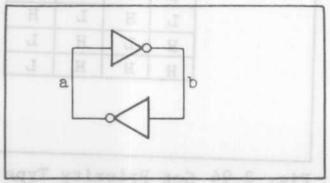


Fig.2-91 Crossed Inverter

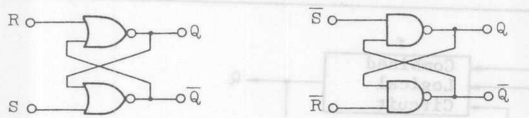
Let us consider the circuit having two stable states. As shown in Fig.2-91, in the circuit where the input and output are connected together, when the point "a" is "H", the point "b" becomes "L", while the point "b" becomes "H" when the point "a" is "L".

Therefore, in both outputs of "a" and "b", the circuit keeps two stable states. However, in this circuit, the state cannot be changed if the circuit is stable in one state.

In the practical use, this strage cell is used as the base to which the circuit for providing memory information is added.

(2) R-S Flip-flop (R-S Latch)

When the crossed inverter is substituted by NAND gate or NOR gate, it



R	S	Q	$\overline{Q}$	
L	L	Q	$\overline{Q}$	Memory
L	H	H	L	
H	L	L	H	
H	H	L	L	Inhibitory condition

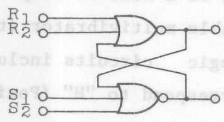
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
L	L	H	H	Inhibitory condition
L	H	H	L	
H	L	L	H	
H	H	Q	$\overline{Q}$	Memory

Fig. 2-92 R-S Flip-Flop

is possible to forcibly decide the memory information.

These circuits shown in Fig. 2-92 are generally called R-S Flip-Flops (or R-S Latches). If the R-S flip-flop is composed of NOR gate, the circuit has memory function with R=S="L".

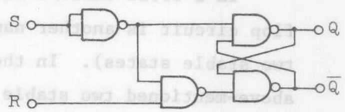
On the basis of basic circuit shown in Fig. 2-92, it is possible to



R	S	Q	$\overline{Q}$
L	L	Q	$\overline{Q}$
L	H	H	L
H	L	L	H
H	H	L	L

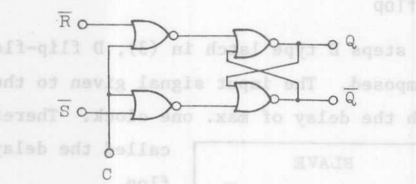
$R = R_1 + R_2$
$S = S_1 + S_2$

Fig.2-93 Multi-input R-S Flip-Flop



S	R	Q	$\overline{Q}$
L	L	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	H	L

Fig. 2-94 Set Priority Type R-S Flip-Flop



C	$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
L	L	L	L	L
L	H	L	H	L
L	L	H	L	H
L	H	H	Q	$\overline{Q}$
H	*	*	Q	$\overline{Q}$

* Don't Care

Fig. 2-95 Gated R-S Flip-Flop

compose the multi-input R-S flip-flop shown in Fig.2-93, set priority R-S flip-flop in Fig. 2-94, and gated R-S flip-flop in Fig. 2-95.

(3) D type latch

Let us again consider the crossed inverter shown in Fig.2-91. In R-S flip-flop, the inversion was made by the substitution to gate IC. However, the circuit for providing input information with switch is considered as shown in Fig. 2-96.

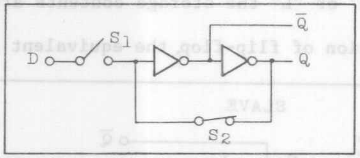
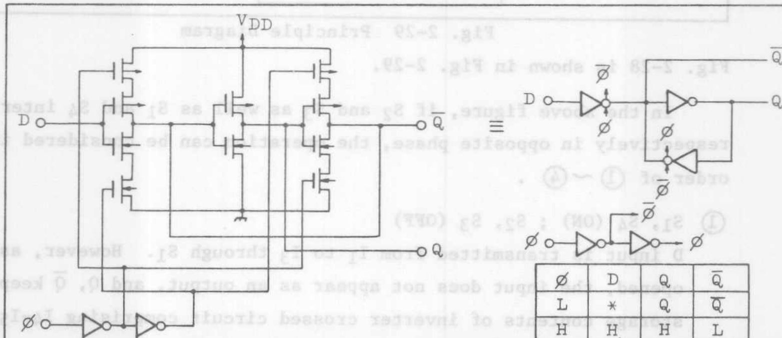


Fig.2-96 Basic D Type Latch

If S_1 and S_2 are always in opposite phase repeating "ON" and "OFF", in the state of S_1 is "ON" and S_2 is "OFF", Q=D, whereby Q output sends D input as it is as the output, which in such a state as S_1 is "OFF" and S_2 is "ON", the input information is stored in the internal circuit.

In C^2MOS IC, similar circuit is accomplished by the method shown in Fig. 2-97 by using clocked inverter instead of S_1 and S_2. This circuit stores information in the state of ϕ = "L".



∅	D	Q	$\overline{Q}$
L	*	Q	$\overline{Q}$
H	H	H	L
H	L	L	H

* Don't Care

Fig. 2-97 D Type Latch by Use of Clocked Inverter

(4) D Type master-slave flip-flop

By connecting by two steps D type latch in (3), D flip-flop in master/slave operation can be composed. The input signal given to the data input appears on the output with the delay of max. one clock. Therefore, this is called the delay type flip-flop.

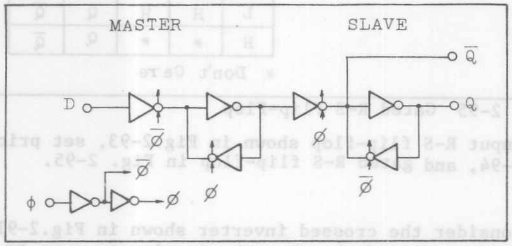


Fig. 2-98 D Type Master-Slave Flip-Flop

Fig. 2-98 shows the basic circuit of D master/slave flip-flop. As is clear from the same figure, the step of master stores information with ϕ = "H", while with ϕ = "L" the step of slave takes over the task of storage, so that without reference to the level of ϕ is "H" or "L" the storage contents are not changed.

For understanding the operation of flip-flop, the equivalent circuit of Fig. 2-28 is shown in Fig. 2-29.

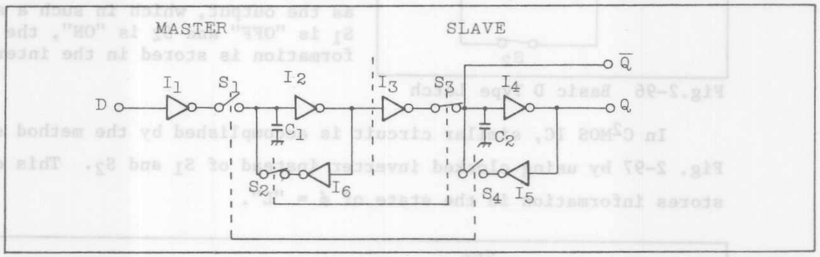


Fig. 2-29 Principle Diagram

In the above figure, if S_2 and S_3 as well as S_1 and S_4 interlock respectively in opposite phase, the operation can be considered in the order of ① ~ ④ .

① S_1, S_4 (ON) ; S_2, S_3 (OFF)

D input is transmitted from I_1 to I_3 through S_1. However, as S_3 is opened, the input does not appear as an output, and Q, $\overline{Q}$ keep the storage contents of inverter crossed circuit comprising I_4-I_5-S_4(ON).

② S_1, S_4 (ON → OFF); S_2, S_3 (OFF → ON)

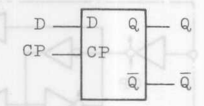
At the step of master, S_2 closes simultaneously with the opening of S_1. Therefore, the memory information of C_1 is kept in the crossed circuit of I_2-I_6-S_2(ON). And at the step of slave, S_3 closes, whereby the information kept in master appears on Q, $\overline{Q}$ outputs. (The information of master renews the information of slave kept previously.)

③ S_1, S_4 (OFF), S_2, S_3 (ON)

The storage is continued in the loop of master, and the output does not change even in the case of change of D input.

④ S_1, S_4 (OFF → ON); S_2, S_3 (ON → OFF)

In the step of slave, S_4 closes simultaneously with the opening of S_3, and the information is stored in the loop of slave. The information was stored in master at the time of ③. Namely, because of no new information, there are no changes in Q, $\overline{Q}$. Further, in the step of master, S_1 closes and S_2 opens, whereby new "D" input is written.



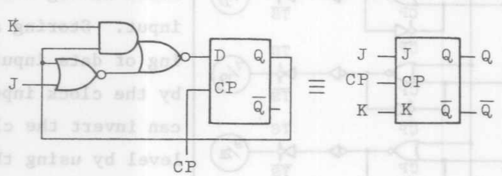
D	CP△	Q	$\overline{Q}$
L	↑	L	H
H	↑	H	L
*	↓	Q	$\overline{Q}$ •

△ Level Change
* Don't Care
• No Change

Fig.2-100 D Type Master-Slave Flip-Flop

Namely, the outputs of Q and $\overline{Q}$ hold D input at that time in transient domain, and the storage is continued until the state of ② occurs again.

Fig. 2-100 shows the block diagram and truth value table of D type master-slave flip-flop.



J	K	CP△	Q	$\overline{Q}$	
L	L	↑	Q	$\overline{Q}$	••
L	H	↑	L	H	
H	L	↑	H	L	
H	H	↑	$\overline{Q}$	Q	•
*	*	↓	Q	$\overline{Q}$	••

△ Level Change, • Change
* Don't Care, •• No Change

Fig.2-101 J/K Master-Slave Flip-Flop

(5) J/K Master-slave flip-flop

Based on D flip-flop, J/K flip-flop can be composed as shown in Fig.2-101.

Table 2-8 List of Latch IC/Flip-Flop IC

Function / No. of Bit	Latch		Flip-Flop	
	D	R - S	D	J / K
2 Bits			TC4013BP	TC4027BP TC7476BP
4 Bits	TC4042BP	TC4043BP TC4044BP	TC40175BP	
6 Bits			TC40174BP	
8 Bits	TC4099BP TC4508BP			

While D flip-flop output is decided by the D input state at the rise time of clock (2 modes), J/K flip-flop output is decided by the combination of J and K (4 modes), whereby J/K master-slave flip-flop is available for wider application as compared with D flip-flop and is extensively used in counter, etc.

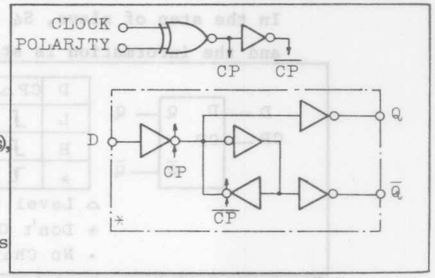


Fig.]-102 TC4042BP (4-Bit "D" Latch)

4.2 Outline of latch IC/ flip-flop IC

(1) D latch

TC4042BP is a 4-bit D latch having common clock input. Storing and rewriting of data input is made by the clock input. TC4042BP can invert the clock level by using the common polarity input. Namely, latch is practicable in both "H" level and "L" level at the clock input.

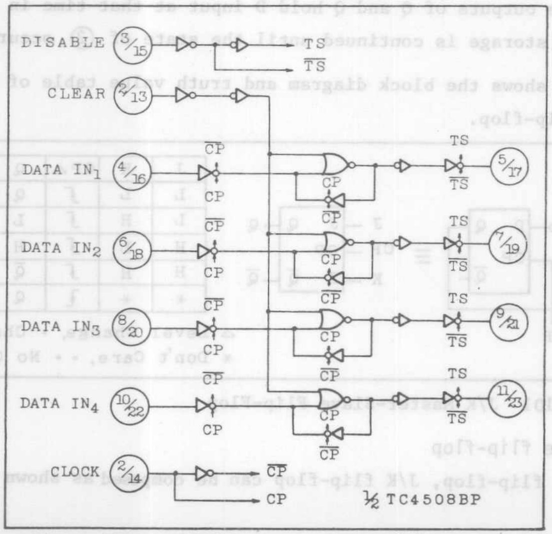


Fig.2-103 TC4508BP Dual 4-Bit "D" Latch

Fig. 2-102 shows the logical diagram of TC4042BP. TC4508BP is a 2-circuit independent 4-bit latch.

Unlike TC4042BP, TC4508BP has no polarity input but is provided with the clear input clearing 4-bit latch and the disable input making the output high impedance, whereby it is possible to perform the Wired-"OR" of output. This function is particularly advantageous in case of time sharing

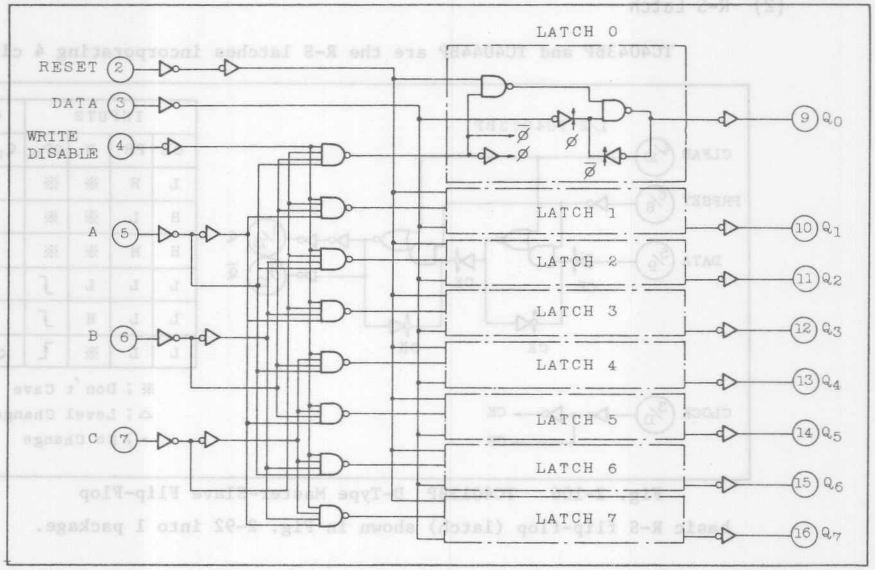


Fig. 2-104 TC4099BP 8-Bit Addressable Latch

desired for the latched output or in case of connecting the latched output to the bus line of microcomputer.

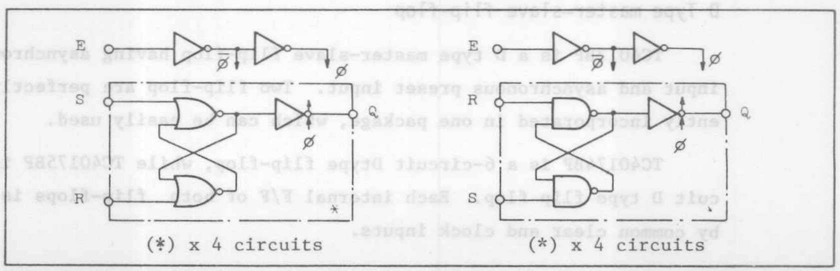
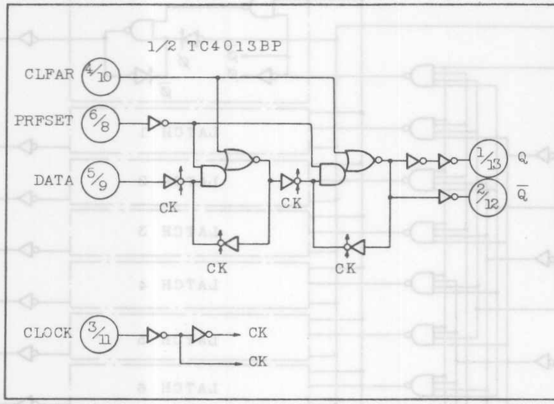


Fig. 2-105 TC4043BP (NOR R-S Latch), TC4044BP (NAND R-S Latch)

Fig. 2-103 shows the logical circuit of TC4508BP. TC4099BP shown in Fig. 2-104 is the addressable latch leading one optional latch out of 8-bit latches to perform storing. In case the number of output ports of microcomputer are insufficient, it is possible to increase the number of output ports by using TC4099BP.

(2) R-S Latch

TC4043BP and TC4044BP are the R-S latches incorporating 4 circuits of



INPUTS				OUTPUTS	
CL	PR	D	CP△	Q_n+1	$\overline{Q}_n+1$
L	R	※	※	H	L
H	L	※	※	L	H
H	H	※	※	L	H
L	L	L	⌠	L	H
L	L	H	⌠	H	L
L	L	※	⌡	Q_n •	$\overline{Q}_n$ •

※ ; Don't Cave
△ ; Level Change
• ; No Change

Fig. 2-106 TC4013BP D-Type Master-Slave Flip-Flop

basic R-S flip-flop (latch) shown in Fig. 2-92 into 1 package.

Fig. 2-105 shows the logic diagrams of TC4043BP and TC4044BP. As is clear from the figure, both TC4043BP and TC4044BP are provided with the common enable input for making the output high impedance.

D Type master-slave flip-flop

TC4013BP is a D type master-slave flip-flop having asynchronous clear input and asynchronous preset input. Two flip-flop are perfectly indenpendently incorporated in one package, which can be easily used.

TC40174BP is a 6-circuit Dtype flip-flop, while TC40175BP is a 4-circuit D type flip-flop. Each internal F/F of both flip-flops is controlled by common clear and clock inputs.

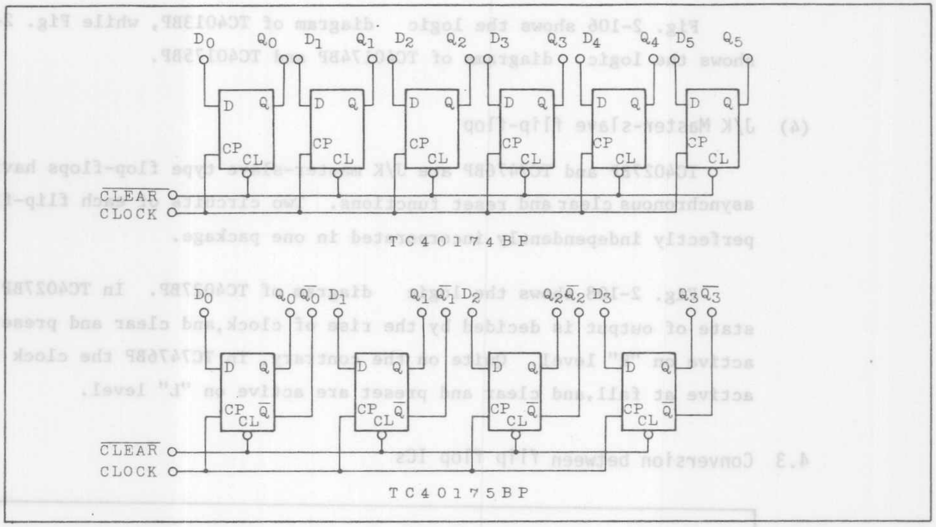
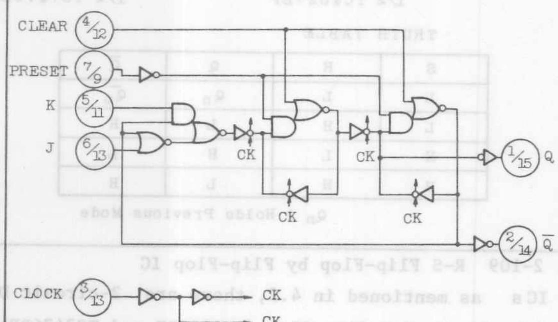


Fig. 2-107 TC40174BP Hex D-Type Flip-Flop
TC40175BP Quad D-Type Flip-Flop



INPUTS					OUTPUTS	
CL	PR	J	K	CP△	Q_n+1	$\overline{Q}_n+1$
L	H	※	※	※	H	L
H	L	※	※	※	L	H
H	H	※	※	※	L	H
L	L	L	L	↑	Q_n	$\overline{Q}_n$ •
L	L	L	H	↑	L	H
L	L	H	L	↑	H	L
L	L	H	H	↑	$\overline{Q}_n$	Q_n ••
L	L	※	※	↓	Q_n	$\overline{Q}_n$ •

※ Don't Care
△ Level Change
• No Change
•• Change

Fig. 2-108 TC4027BP J/K Master-Slave Flip-Flop

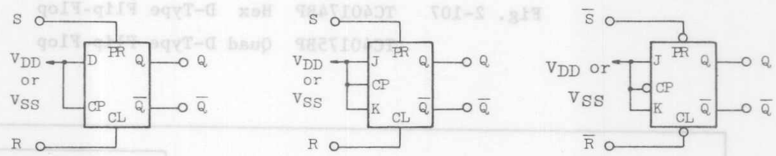
Fig. 2-106 shows the logic diagram of TC4013BP, while Fig. 2-107 shows the logic diagrams of TC40174BP and TC40175BP.

(4) J/K Master-slave flip-flop

TC4027BP and TC7476BP are J/K master-slave type flop-flops having asynchronous clear and reset functions. Two circuits of each flip-flop are perfectly independently incorporated in one package.

Fig. 2-108 shows the logic diagram of TC4027BP. In TC4027BP the state of output is decided by the rise of clock,and clear and preset are active on "H" level. Quite on the contrary, in TC7476BP the clock is active at fall,and clear and preset are active on "L" level.

4.3 Conversion between flip flop ICs



1/2 TC4013BP 1/2 TC4027BP 1/2 TC7476BP

TRUTH TABLE

S	R	Q	$\overline{Q}$
L	L	Q_n	$\overline{Q}_n$
L	H	L	H
H	L	H	L
H	H	L	H

Q_n ; Holds Previous Mode

Fig. 2-109 R-S Flip-Flop by Flip-Flop IC

In flip-flop ICs as mentioned in 4.2, there are 2-circuit D flip-flop (TC4013BP) and 2-circuit J-K flip-flop (TC4027BP and TC7476BP). In case any other flip-flop is desired, it is possible to readily compose such flip-flop by using D flip-flop and J-K flip-flop.

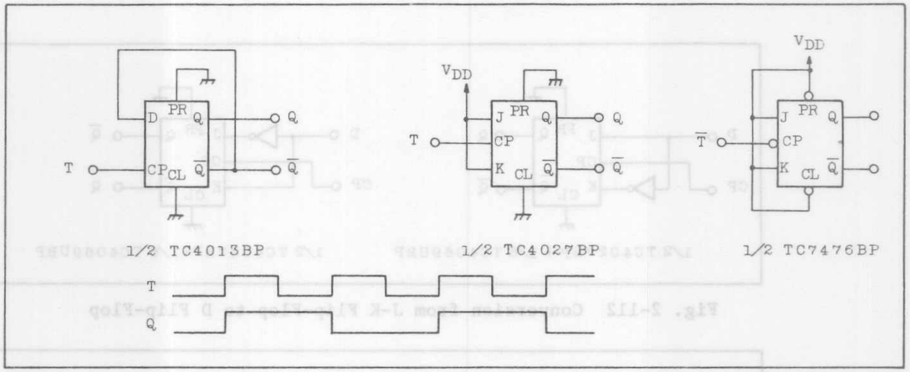


Fig. 2-110 T Flip/Flop by Flip-Flop IC

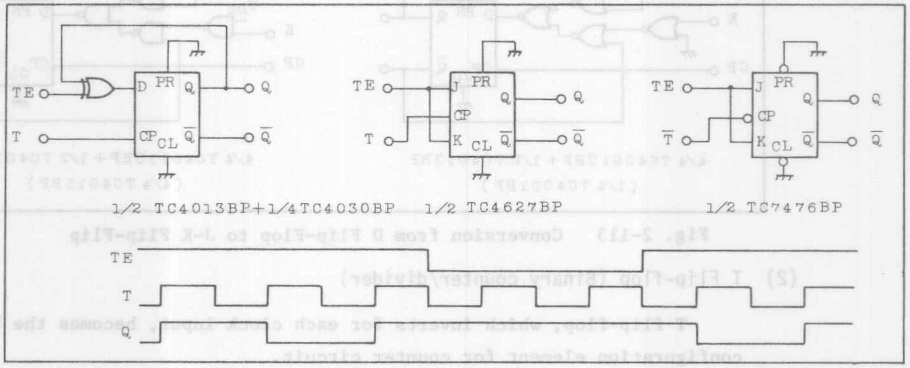


Fig. 2-111 T Flip/Flop with controlling Input by Flip-Flop IC

For example, the use of gate IC makes it possible to perform the conversion between J-K flip-flop and D flip-flop, whereby the surplus flip-flop in the circuit can be converted to any other type.

(1) R-S Flip-flop

By using clear (CLEAR) input and preset (PRESET) input of TC4013BP, TC4027BP and TC7476BP, R-S flip-flops can be constructed. However, in case both R input and S input have become ENABLE, unlike the R-S flip-flop composed by gate IC, priority is given to R input.

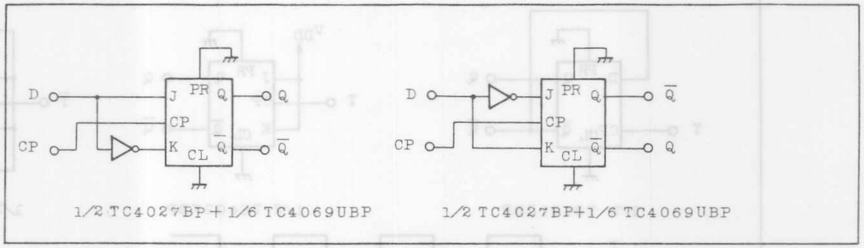


Fig. 2-112 Conversion from J-K Flip-Flop to D Flip-Flop

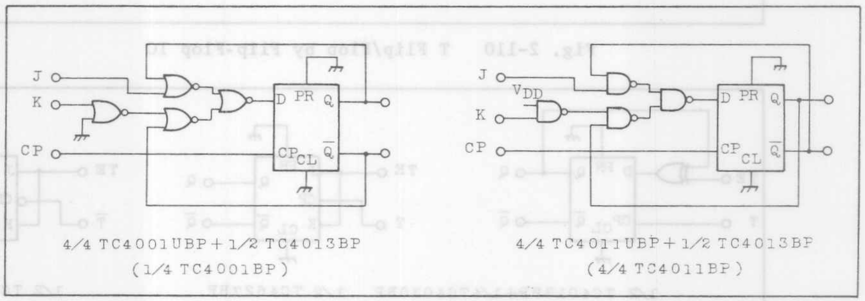


Fig. 2-113 Conversion from D Flip-Flop to J-K Flip-Flip

(2) T Flip-flop (Binary counter/divider)

T flip-flop, which inverts for each clock input, becomes the basic configuration element for counter circuit.

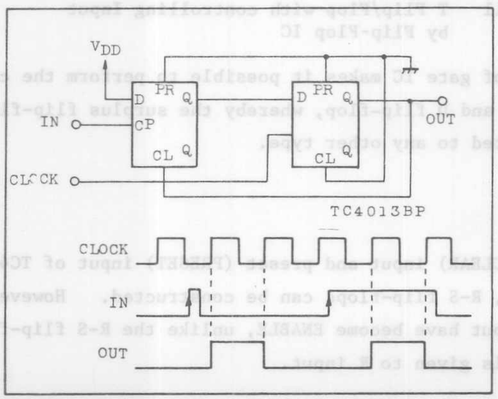


Fig. 2-114 Pulse Synchronizer (a)

In the T flip-flop, there are two types, one being the type of unconditionally inverting when the clock enters and the other being the type capable of selecting inversion and non-inversion according to the state of TE (Toggle enable).

Fig. 2-110 and Fig. 2-111 show the examples of the connection of T flip-flops. In the same figures, PRESET input and CLEAR input are processed. In usual circuits, however, they are often connected to other circuits for initializing or state setting at optional time.

(3) Mutual conversion between D flip-flop and J-K flip-flop

In case TC4013BP is desired to be used like TC4027BP or TC7476BP; or on the contrary, in case TC4027BP and TC7476BP are desired to be used like TC4013BP, the conversion is easily practicable by putting gate IC externally.

Fig. 2-112 shows an example of the use of J-K flip-flop as D flip-flop, while Fig. 2-113 shows an example of the use of D flip-flop as J-K flip-flop.

4.4 Flip-flop/latch application circuits

(1) Pulse synchronizer (a)

Fig. 2-114 shows a pulse synchronizer synchronizing the signal input at random by the clock of system.

In this circuit, whenever there is a rise of input signal irrespective of length of input signal, the pulse corresponding to one cycle of clock is made by catching the rise edge of input signal. Further, during the rise of output, the preceding step of F/F is reset, whereby other inputs are inhibited to prevent mulfunctions, such as chattering, etc.

(2) Pulse synchronizer (b)

Like (1), Fig. 2-115 shows the circuit for synchronizing the input signals entering with the asynchronous state with the clock.In the case of this circuit, it is possible consicerably to remove chattering by setting the frequency of clock properly. However, for reliabler operation, (II) three-step system is more effective than (I) two-step system.

(3) Frequency divider by Johnson counter system

Johnson counter is accomplished by connecting D flip-flop in a shift register form and connecting the inversion output of the last step to the data input of the initial step. The special characteristics of this counter are that the whole output is obtainable at 50% duty cycle and no hazard appears in case whatever gate is added to the output.

Fig. 2-116 shows an example of a 1/4-frequency divider, while Fig.

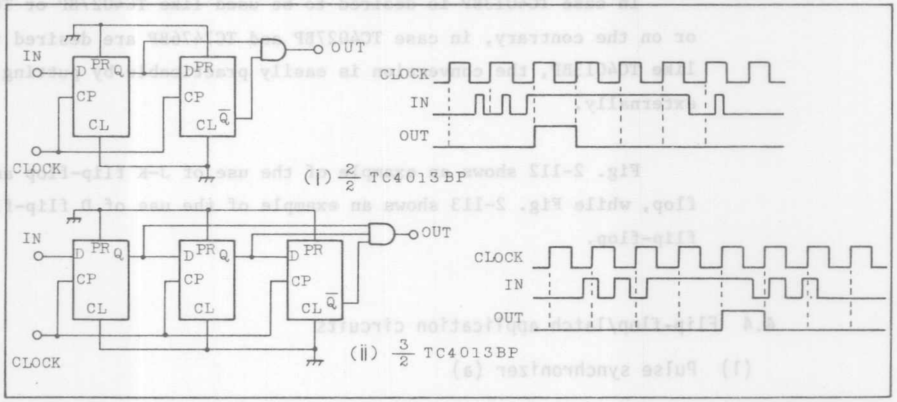


Fig. 2-115 Pulse Synchronizer (2)

2-117 shows an example of a 1/6 frequency divider.

In case no gate is added to the frequency divider shown in Fig. 2-117, when the power is turned on, or the flip-flop becomes the state Q_A = "H", Q_B = "L", and Q_C = "H" by the external noises, in the next clock, the flip-flop becoems the state Q_A = "L", Q_B = "H", and Q_C = "L", in the second clock, the flip-flop returns to the original state; thus the reciprocation is made between two modes of "H"-"L"-"H" and "L"-"H"-"L", and division of frequency is not expected.

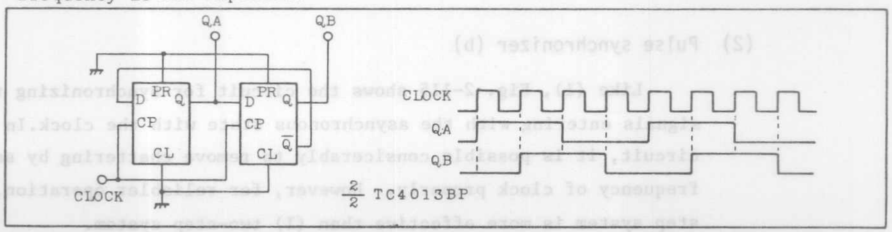


Fig. 2-116 1/4-Frequency Divider

In the mode other than the normal counting work, in case there is any closed loop not returning to the original, this loop is generally called labyrinth loop.

In Fig. 2-117, the gate is installed so that the labyrinth loop may automatically return to the normal count.

In general, at the time of designing the counter and divider, consideration is required so as not to cause the labyrinth loop.

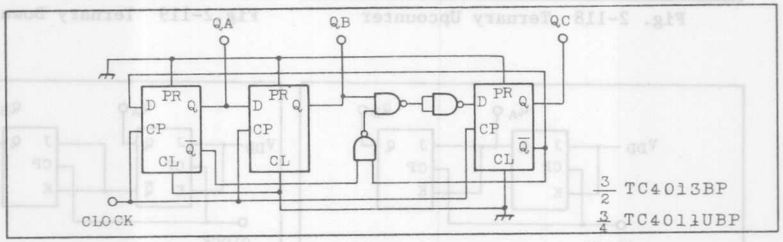


Fig. 2-117 1/6 Frequency Divider

By the same procedure, the circuits for 8 dividing and 10 dividing can be realized. In this case, however, it is advantageous to use TC4018BP or TC4022BP and TC4017BP of MSI.

(4) Synchronous type N up-and-down counter (ternary ~ hexadecimal)

By using J/K flip-flop, various counters can be composed. Here, by using TC4027BP (and some gate ICs), introduction is made from synchronous type ternary-up-counter to hexadecimal-down-counter.

Examples of connections of various counters are shown in Fig.2-118 to Fig.2-145. In the figures, CLEAR and PRESET of TC4027BP are all omitted; therefore, CLEAR and PRESET shall be all processed as GND (V_{SS}). Count sequence is described in all the drawings.

Namely, each flip-flop composing the counters is given weight 1-2-4-8 from the initial step, and all of the logical state forming the counters are expressed by decimal. The mode other than normal count mode shown by full line arrow mark returns to the normal loop as shown by dashed line.

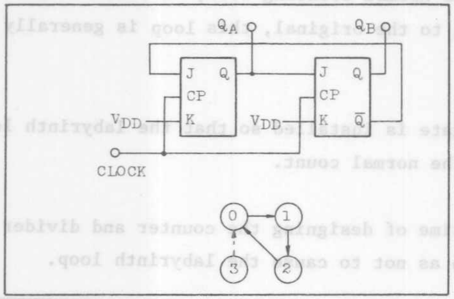


Fig. 2-118 Ternary Upcounter

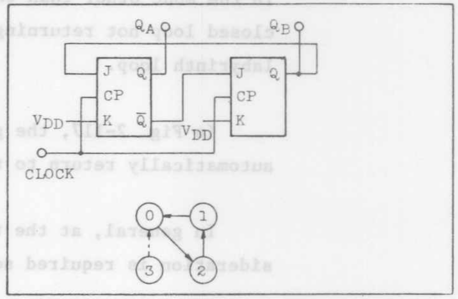


Fig.2-119 Ternary Downcounter

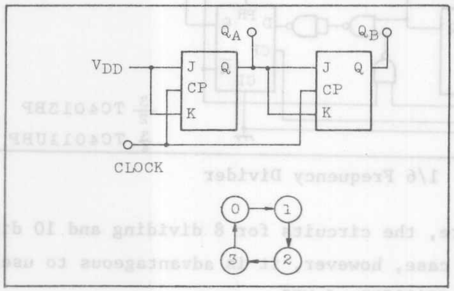


Fig. 2-120 Quadrinary Upcounter

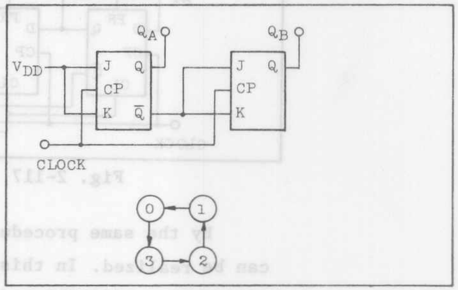


Fig. 2-121 Quadrinary Downcounter

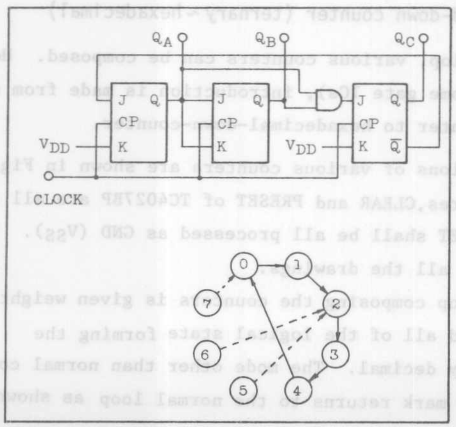


Fig. 2-122 Quinary Upcounter

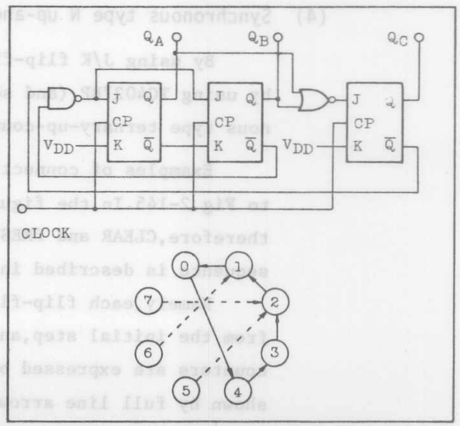


Fig. 2-123 Quinary Dowuncounter

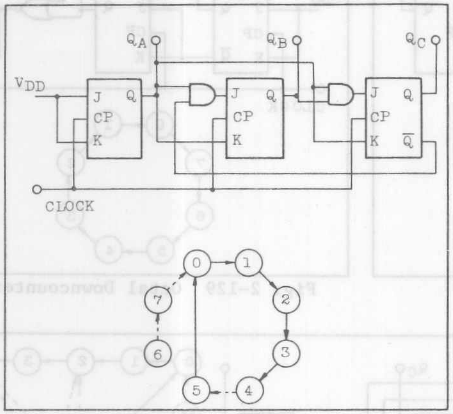


Fig. 2-124 Sexinary Upcounter

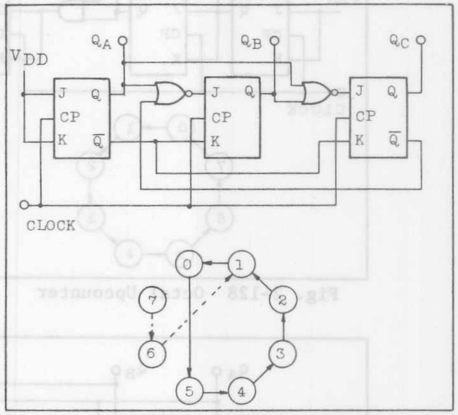


Fig. 2-125 Sexinary Downcounter

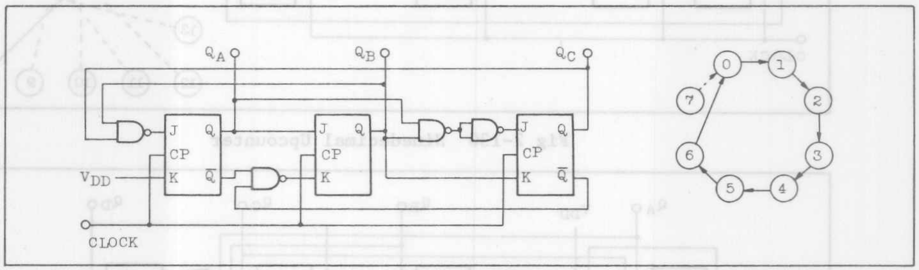


Fig. 2-126 Heptanary Upcounter

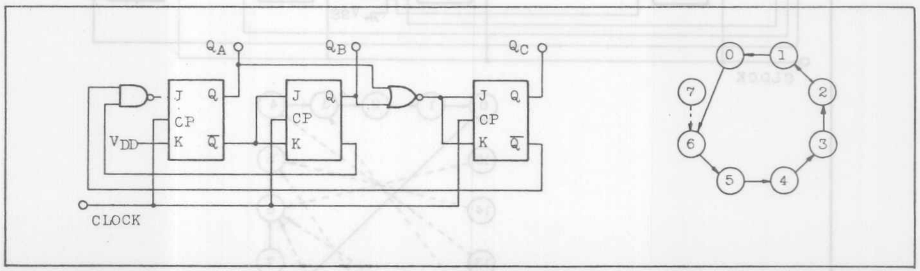


Fig. 2-126 Heptanary Downcounter

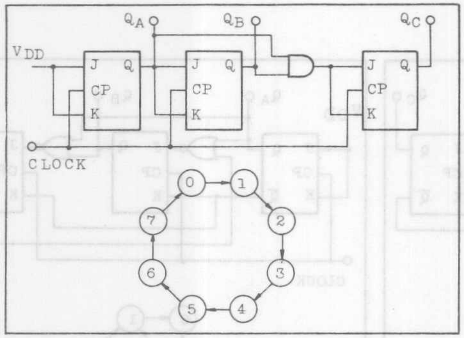


Fig. 2-128 Octal Upcounter

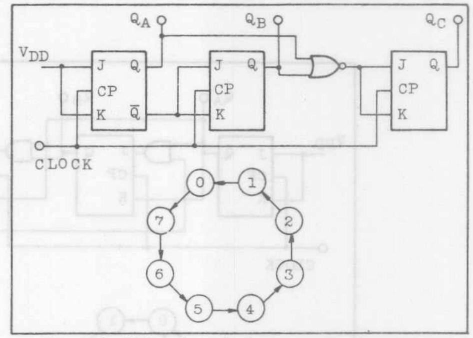


Fig. 2-129 Octal Downcounter

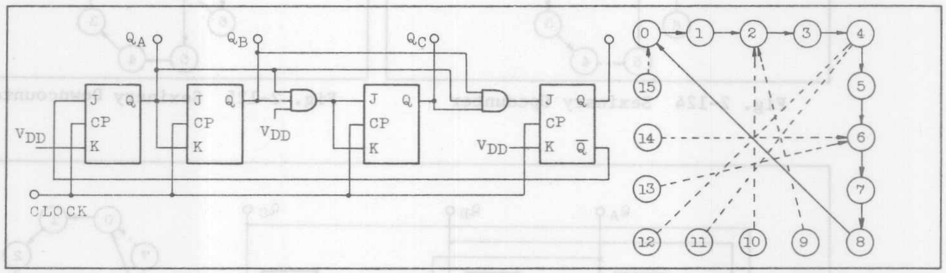


Fig 2-130 Ninedecimal Upcounter

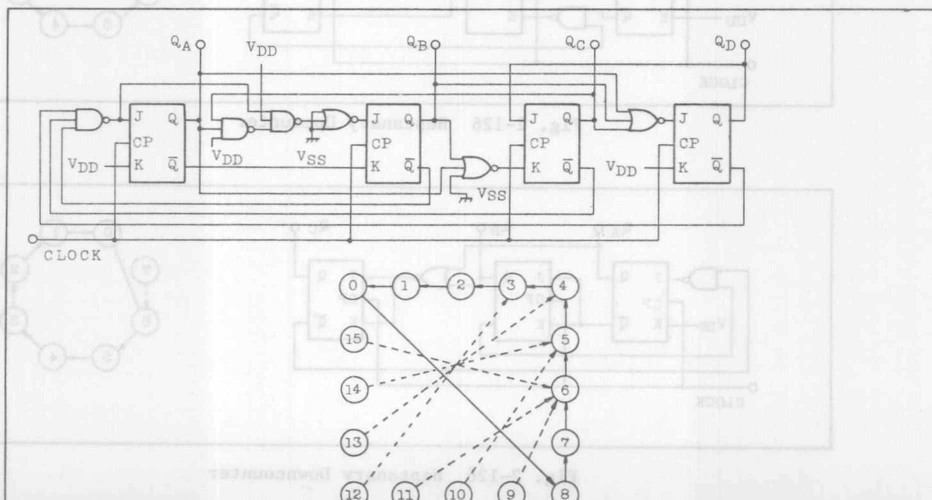


Fig. 2-131 Ninedecimal Downcounter

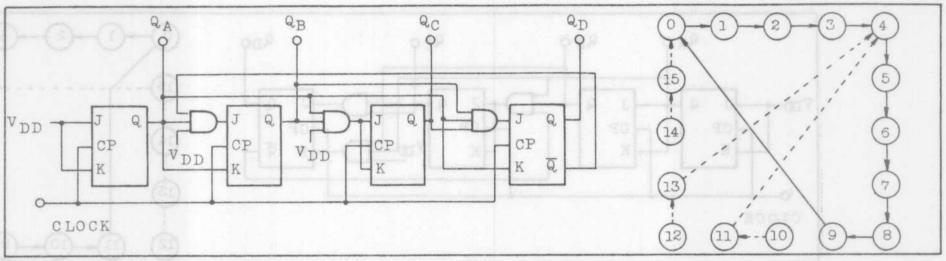


Fig. 2-132 Decimal Upcounter

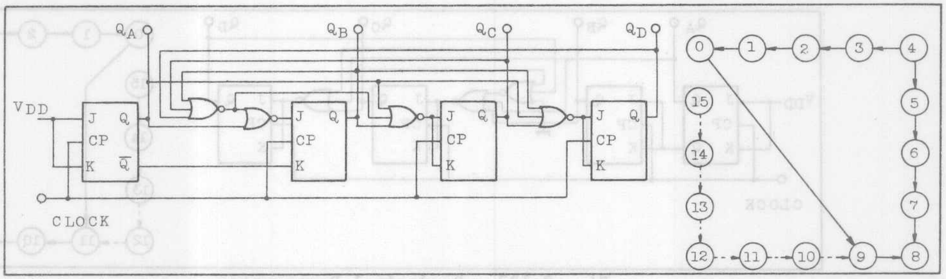


Fig. 2-133 Decimal Downcounter

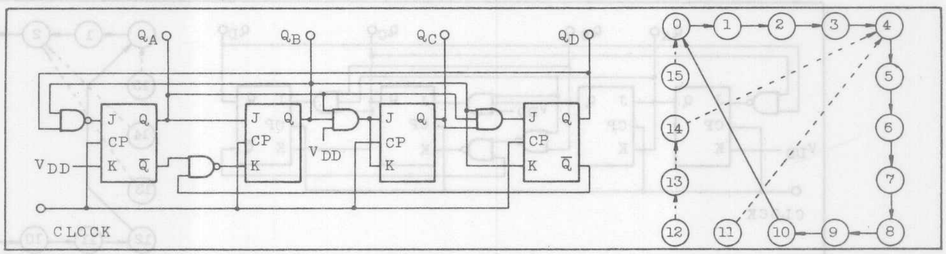


Fig. 2-134 Onedecimal Upcounter

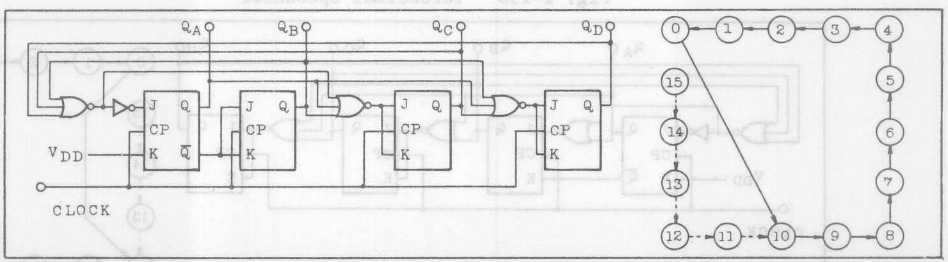


Fig. 2-135 Onedecimal Downcounter

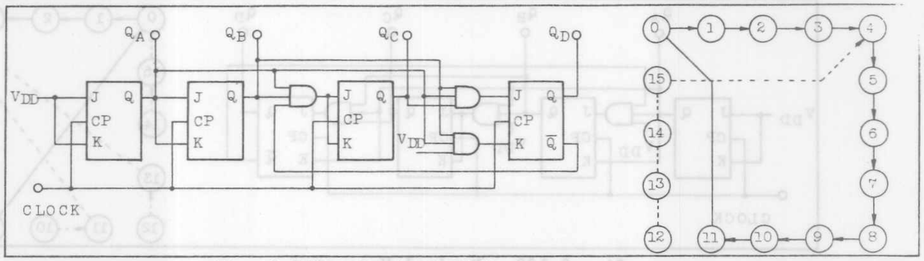


Fig. 2-136 Duodecimal Upcounter

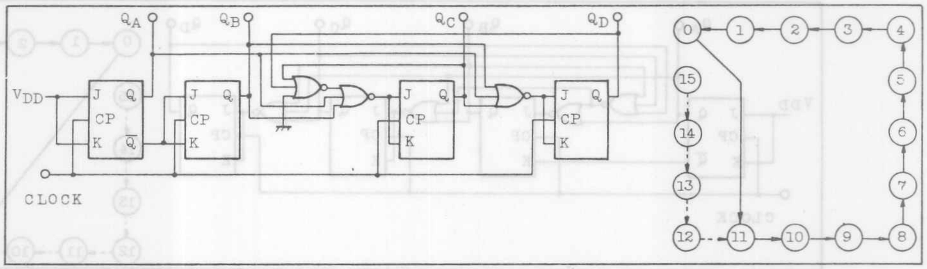


Fig. 2-137 Duodecimal Downcounter

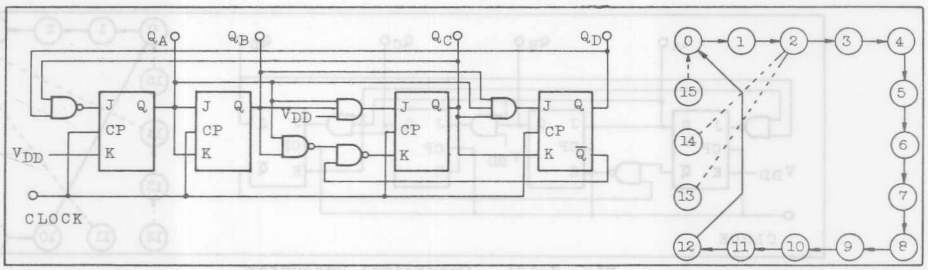


Fig. 2-138 Terdecimal Upcounter

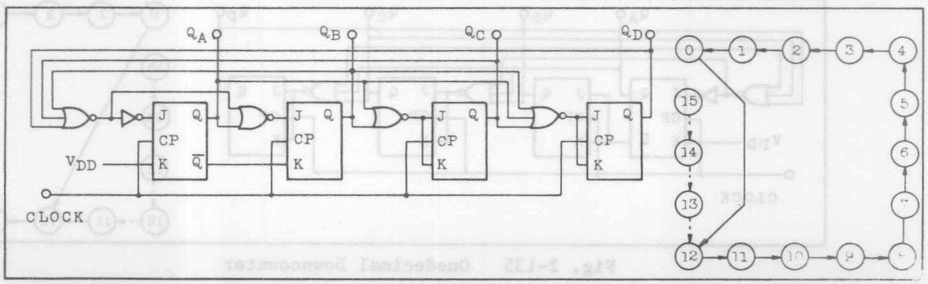


Fig. 2-139 Terdecimal Downcounter

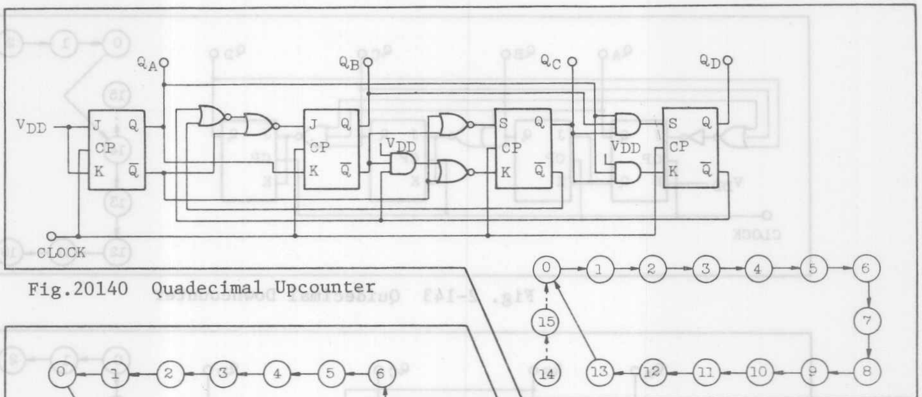


Fig.20140 Quadecimal Upcounter

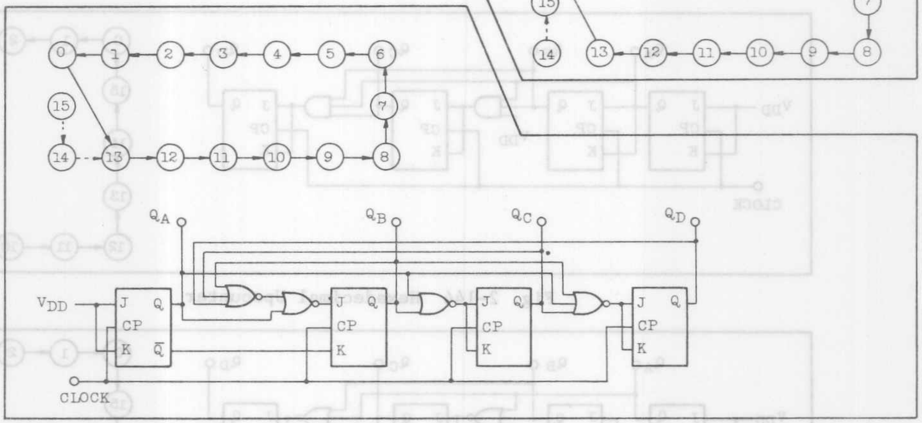


Fig. 2-141 Quadecimal Downcounter

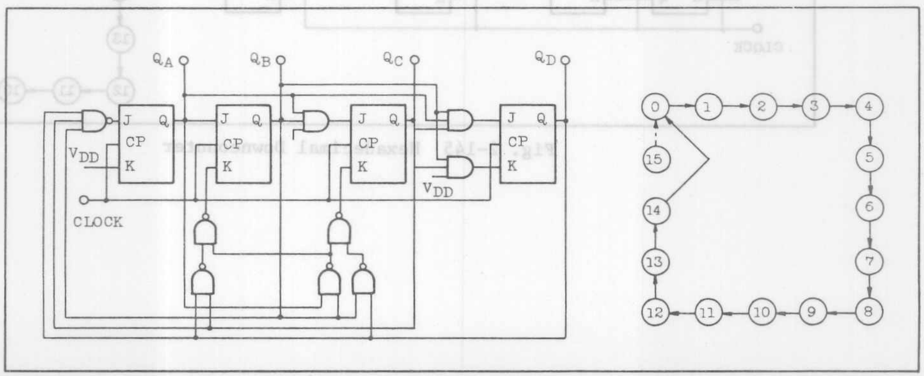


Fig. 2-142 Quidecimal Upcounter

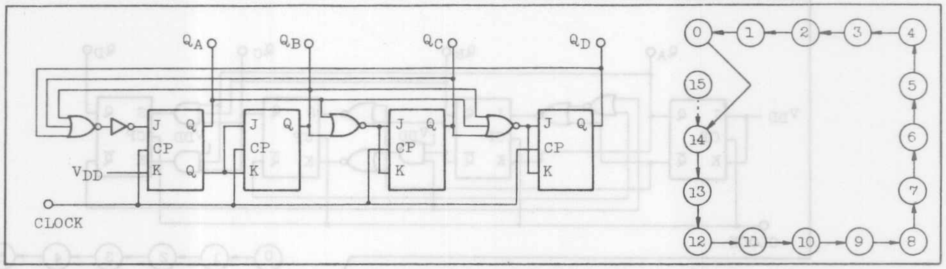


Fig. 2-143 Quidecimal Downcounter

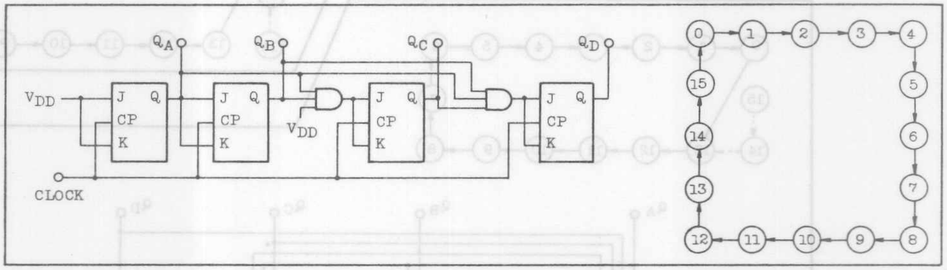


Fig. 2-144 Hexadecimal Upcounter

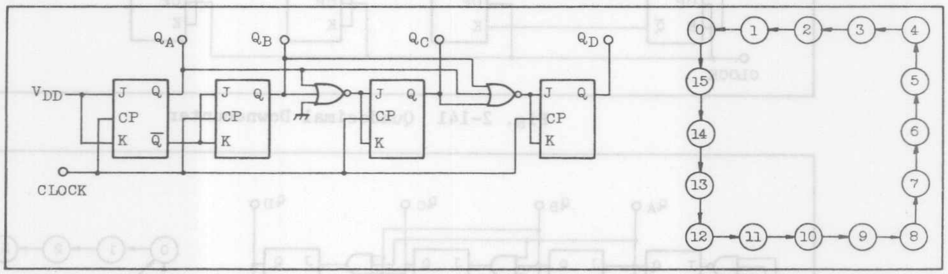
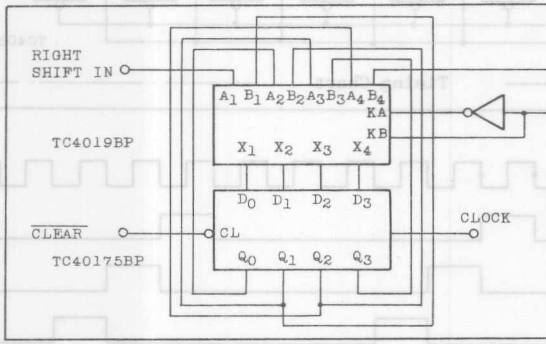


Fig. 2-145 Hexadecimal Downcounter

(5) 4-Bit bidirectional shift register

If connection is made as shown in Fig.2-146 by using TC40175BP and TC4019BP(Quad AND/OR Select Gate), it is possible to realize the bidirectional shift register capable of both right shift and left shift.

Further, by cascading this basic circuit, it is easy to compose 8 bits and 16 bits.



FUNCTIONAL TABLE

$\overline{CL}$	L/R	CP	MODE
L	※	※	CLEAR
H	※	⌐	NO CHANGE
H	H	⌐	SHIFT LEFT
H	L	⌐	SHIFT RIGHT

Fig. 2-146 4-Bit Right Shift/Left Register

(6) Ring counters

The ring counter, in which "H" level or "L" level pulses shift in order according to the clock input, is the circuit having very extensive uses. In the ring counters introduced here, the shift register is composed by using TC40174BP or TC40175BP.

Fig. 2-147 shows the ring counter with the output being available at "H" level active, while Fig. 2-148 shows the ring counter with the output being available at "L" level active.

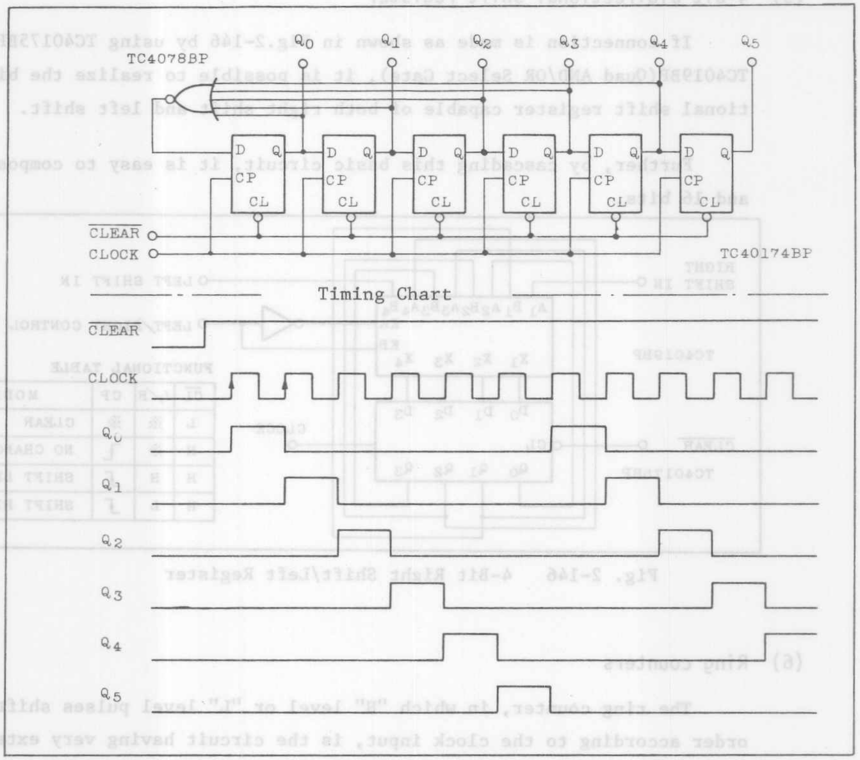


Fig. 2-147 6-State Ring Counter ("H" level active)

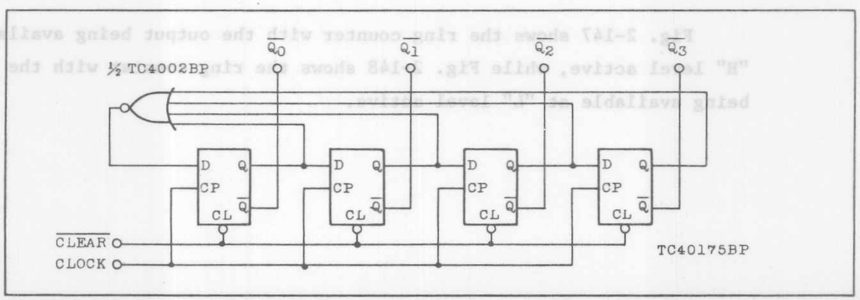


Fig. 2-148 4-State Ring Counter ("L" level active)

(7) Three-state connection

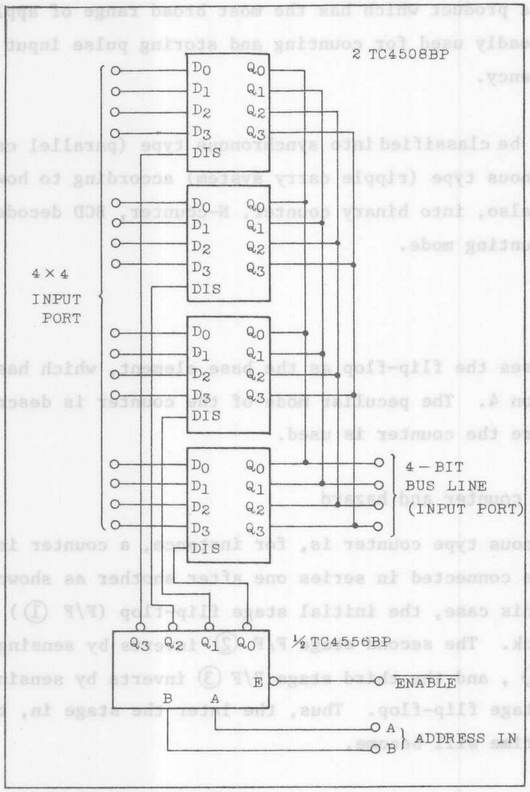


Fig.2-149 Expansion of Input Port by TC4508BP

TC4508BP is capable of making the output high impedance by using the disable input. By using this function, three-state connection is practicable by connecting output to output.

Fig. 2-149 shows the circuit for riding 16-bit input signal on bus line or input port of microcomputer by using two devices of TC4508BP. In general, general-purpose processor, such as microcomputer, is provided with a fixed amount of ports only. This circuit is effective when the expansion of input port is desired.

5. Counter

The counter is a product which has the most broad range of application among MSI, and is broadly used for counting and storing pulse input and for dividing input frequency.

The counter may be classified into synchronous type (parallel carry system) and asynchronous type (ripple carry system) according to how clock input is given, and also, into binary counter, N-counter, BCD decode counter etc. according to counting mode.

5.1 Counter circuit

The counter uses the flip-flop as the base element, which has been described in Section 4. The peculiar mode of the counter is described in the following before the counter is used.

(1) Asynchronous type counter and hazard

The asynchronous type counter is, for instance, a counter in which the flip-flops are connected in series one after another as shown in Fig. 2-150. In this case, the initial stage flip-flop (F/F ①) is inverted by the clock. The second stage F/F ② inverts by sensing change in output from F/F ①, and the third stage F/F ③ inverts by sensing output from the second stage flip-flop. Thus, the later the stage in, the larger the delay time will become.

The delay time between the flip-flop clock and output $\bar{Q}$ is specified in the catalog. When this value is assumed to be t_{pd}. The delay time of output from clock input to n-th stage is n x (t_{pd}).

If it is assumed that a gate detecting arbitrary counting state is added by structuring, an octal up-counter using this asynchronous counter, odd number detection output (e.g. "7") can be normally obtained, but hazard is generated on even number detection output (e.g., "6").

In this way, the asynchronous type counter may not function properly if the logic process of its output is easily carried out.

On the synchronous type actal counter shown in Fig. 2-151, no hazard is generated even when a gate is added similarly. This is because the clock is applied in parallel to each F/F structuring the counter, and is more advantageous for generating control pulse ($Q_A \cdot Q_B \cdot Q_C$, $\overline{Q_A} \cdot Q_B \cdot Q_C$ in Fig. 2-150) than the circuit shown in Fig. 2-150.

Therefore, with the exception of a simple frequency division circuit, the asynchronous type counter is not often used. When asynchronous type counter (e.g., TC4024BP, TC4020BP or TC4040BP) is used, care must be exercised so that these hazards do not occur.

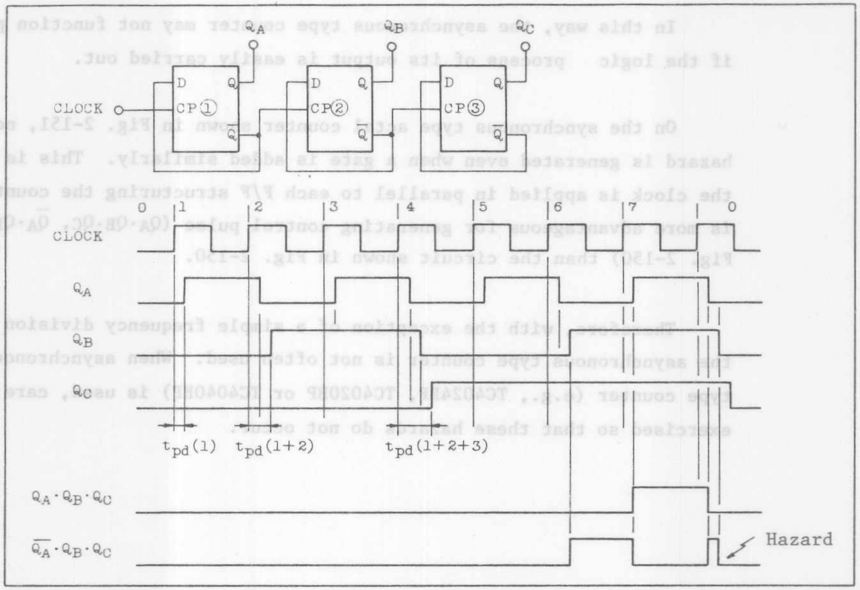


Fig. 2-150 Asychronous Type Octal Counter

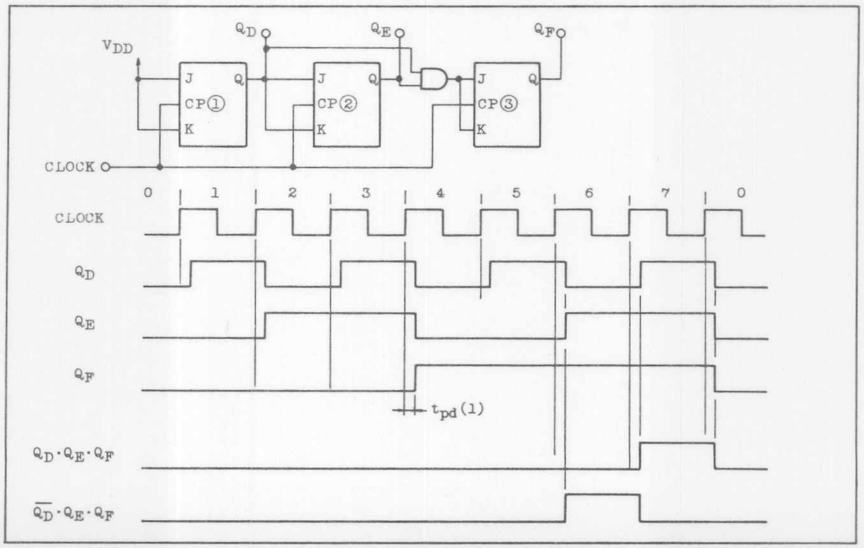


Fig. 2-151 Synchronous Type Octal Counter

(2) Counter and loop

The counter is basically composed of several flip-flops (F/F). As these F/Fs function as the information storage elements of the counter, for n-counter, n-F/Fs satisfying

$$2^{n-1} < N \leqq 2^n \quad \text{(n: integral number)}$$

are required.

That is, on a quinary counter

$$2^2 < 5 < 2^3$$

Therefore, n = 3, and 3 F/Fs are required.

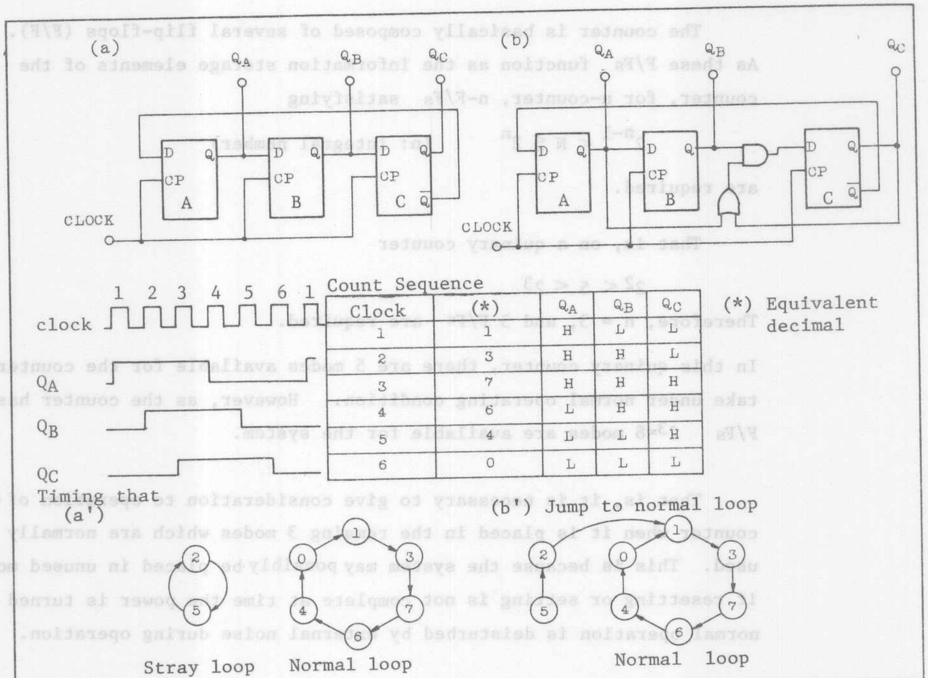
In this quinary counter, there are 5 modes available for the counter to take under normal operating condition. However, as the counter has 3 F/Fs $2^3=8$ modes are available for the system.

That is, it is necessary to give consideration to operation of the counter when it is placed in the remaing 3 modes which are normally not used. This is because the system may possibly be placed in unused mode if resetting or setting is not complete at time the power is turned on or normal operation is deisturbed by external noise during operation.

In the next, the loop is explained using 2-sexinary shift counters shown in Fig. 2-152. Both circuits (a) and (b) in Fig. 2-152 operate as sexinary counters shown in the count sequence.

Now, if the counting state is shown giving weight "1", "2" and "4" to each of F/Fs composing the circuit in the sequence of A, B, and C, operating of respective counters (a) and (b) can be shown in Fig. (a') and (b').

In this case, a stray loop where states "2" and "5" invert each other exists in (a') in addition to the normal count loop. Because of this stray loop, if the frequency division circuit is placed in this mode, permanent division of frequency into 1/6 becomes impossible.



Count Sequence

Clock	(*)	Q_A	Q_B	Q_C
1	1	H	L	L
2	3	H	H	L
3	7	H	H	H
4	6	L	H	H
5	4	L	L	H
6	0	L	L	L

(*) Equivalent decimal

Fig. 2-152 Loop Analysis

On the other hand, this stray loop does not exist in (b') as a jump circuit which is provided to restore the circuit to the normal loop immediately from this mode.

Therefore, it can be said that the circuit (b) is better than (a). In general, in structuring a counter system it is necessary to make sure in advance that there is no abnormal loop in the circuit.

5.2 Type of Counter

The counter of C^2MOS IC has most many versions among C^2MOS MSI/LSI. Shown in Table 2-9 is a table of the asynchronous binary counters.

Those frequency dividing outputs with "O" mark in the table can be taken out from each output pin. Further, TC4024BP, TC4020BP and TC4040BP have no oscillation circuits, and TC4521BP, TC5036P and TC5048P are built-in oscillation circuit types.

TC5036P and TC5048P are dynamic types in circuits up to the fourth stage and frequency division up to 8 MHz at 5V is possible.
Shown in Table 2-10 is a table of the synchronous counters.

The synchronous counters may be classified into binary counter decimal counter, BCD decode counter, N-counter, etc. Further, as up/down count selectable type and presettable type counters are available in addition to a counter that is used for simple up-counting only, it is necessary properly to select counters that have expected functions.

Table 2-9 Asynchronous Binary Counters

Type	Output Pin																								Circuit type
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}	Q_{16}	Q_{17}	Q_{18}	Q_{19}	Q_{20}	Q_{21}	Q_{22}	Q_{23}	Q_{24}	
TC4024BP	○	○	○	○	○	○	○	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Static
TC4020BP	○	—	—	○	○	○	○	○	○	○	○	○	○	○	—	—	—	—	—	—	—	—	—	—	Static
TC4040BP	○	○	○	○	○	○	○	○	○	○	○	○	—	—	—	—	—	—	—	—	—	—	—	—	Static
TC4521BP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	○	○	○	○	○	○	○	Static
TC5036 P	—	—	—	△	—	—	—	—	□	—	—	○	○	○	○	○	○	—	—	—	—	—	—	—	Dynamic
TC5048 P	—	—	—	△	○	○	○	—	□	—	—	—	—	○		○	○	—	—	—	—	—	—	—	Dynamic

Note) △ ; duty cycle 34.4%

□ ; frequency check output

Table 2-10 Synchronous Counters

Function		Up	Up/Down	Presettable Up	Presettable Up/Down	Other
Binary	4 bits	TC5027BP		TC40161BP TC40163BP	TC4516BP TC4029BP	TC5018P
Binary	2x4 bits	TC4520BP				
Octal		TC4022BP				
Decimal		TC4017BP				
BCD Decode	1 digit	TC5026BP		TC40160BP TC40162BP	TC4510BP TC4029BP	
BCD Decode	2 digits	TC4518BP				
BCD Decode	4 digits	TC5001 P TC5037 P TC5051 P TC5052 P	TC5010P	No applicable product		
BCD Decode	6 digits	TC5032 P				
N-counter		TC4018BP				

(1) Ripple carry binary counter

TC4024BP, TC4040BP, and TC4020BP are ripple carry binary counters that have master-slave D-flip-flops connected in sequence as illustrated in Fig. 2-153 ~ Fig. 2-155. All of the flip-flops can be reset to "0" by CLEAR input.

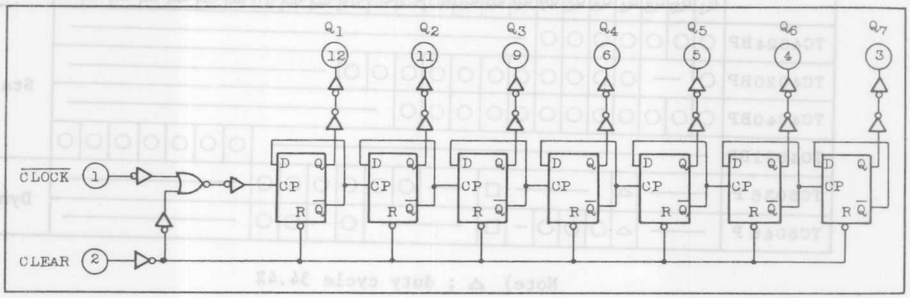


Fig. 2-153 TC4024BP 7 STAGE RIPPLE CARRY BINARY COUNTER

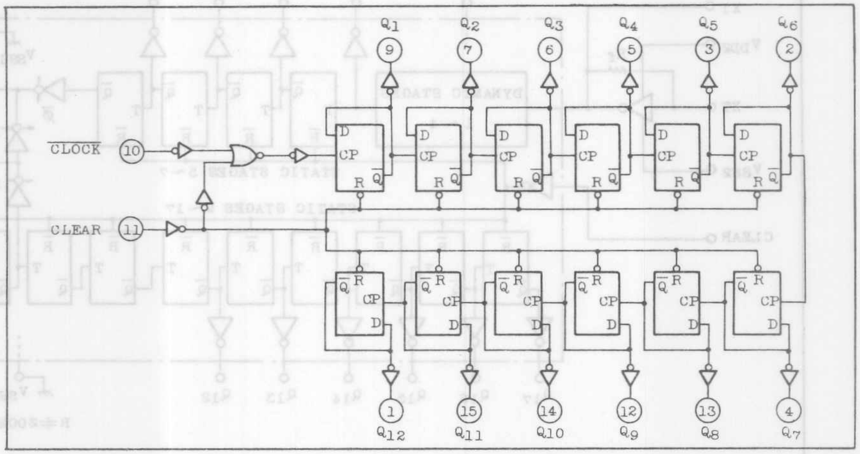


Fig. 2-154   TC4040BP   12 STAGE RIPPLE CARRY BINARY COUNTER

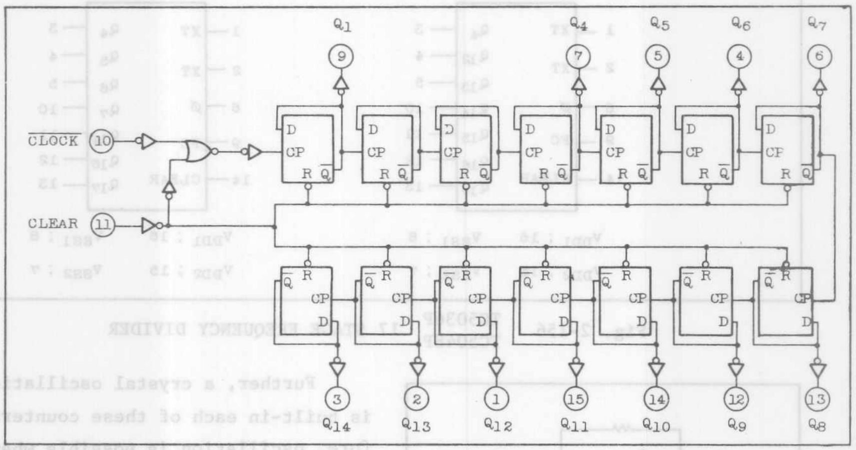


Fig. 2-155   TC4020BP   14 STAGE RIPPLE CARRY BINARY COUNTER

TC5036P and TC5048P illustrated in Fig. 2-156 are 17-stage high-speed ripple carry binary counters. As the flip-flops up to fourth stage are of dynamic configuration, clock inputs up to 8 MHz can be divided at 5V. Frequency division at f_{MIN} (20 KHz) or below, however, is not guaranteed.

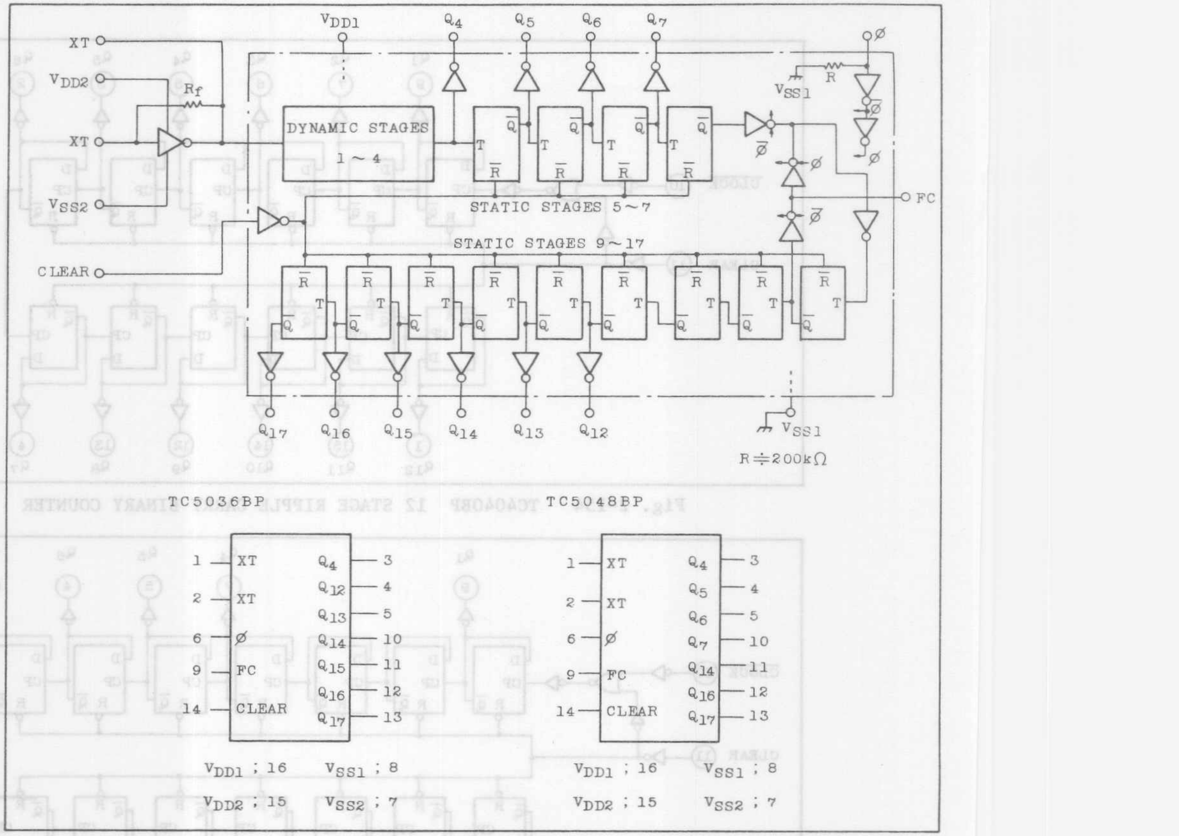


Fig. 2-156 TC5036P TC5048P 17 STAGE FREQUENCY DIVIDER

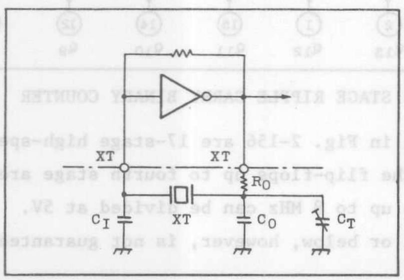


Fig.2-157 Example of Crystal Oscillation Circuit

Further, a crystal oscillation inverter is built-in each of these counters; therefore, oscillation is possible when the crystal is connected to X_T and $\overline{X}_T$ terminals as shown in Fig.2-157. However, since no specified accuracy including constant and crystal that is used in a clock frequency divider has been guaranteed, oscillation may not be obtained even in the operating of counter depending upon a crystal and C_I/C_O being used.

Therefore, it may be essential to check stabilized oscillation in advance using a crystal to be used.

Illustrated in Fig. 2-158 is TC4521BP ripple carry binary counter containing 24-stage static flip-flops. TC4521BP has the crystal oscillation inverter and RC oscillation circuit inserted into the input and either of them is capable of generating oscillation pulse.

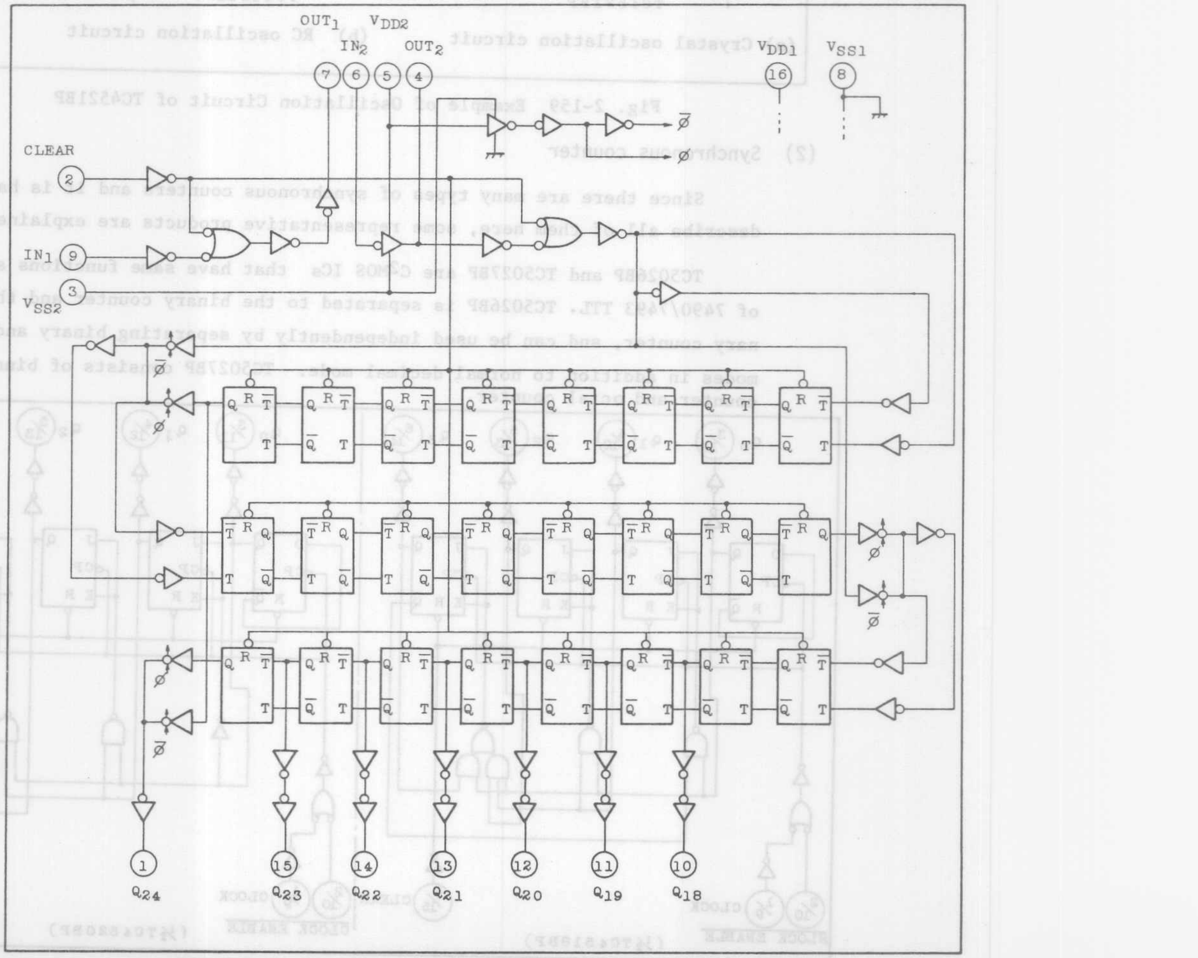


Fig. 2-158 TC4521BP 24 STAGE FREQUENCY DIVIDER

An example of the oscillation circuit of TC4521BP is illustrated in Fig.2-159.

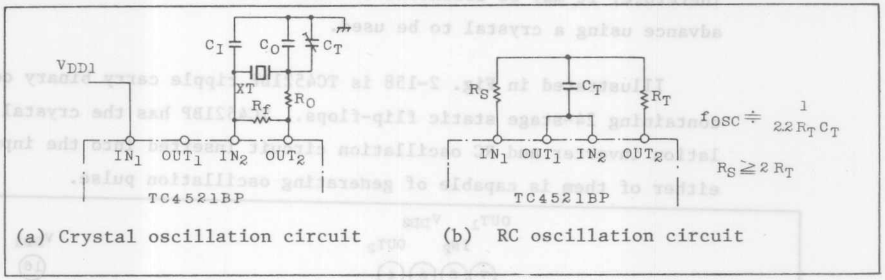


Fig. 2-159 Example of Oscillation Circuit of TC4521BP

(2) Synchronous counter

Since there are many types of synchronous counters and it is hard to describe all of them here, some representative products are explained.

TC5026BP and TC5027BP are C^2MOS ICs that have same functions as those of 7490/7493 TTL. TC5026BP is separated to the binary counter and the quinary counter, and can be used independently by separating binary and quinary modes in addition to normal decimal mode. TC5027BP consists of binary counter and octal counter.

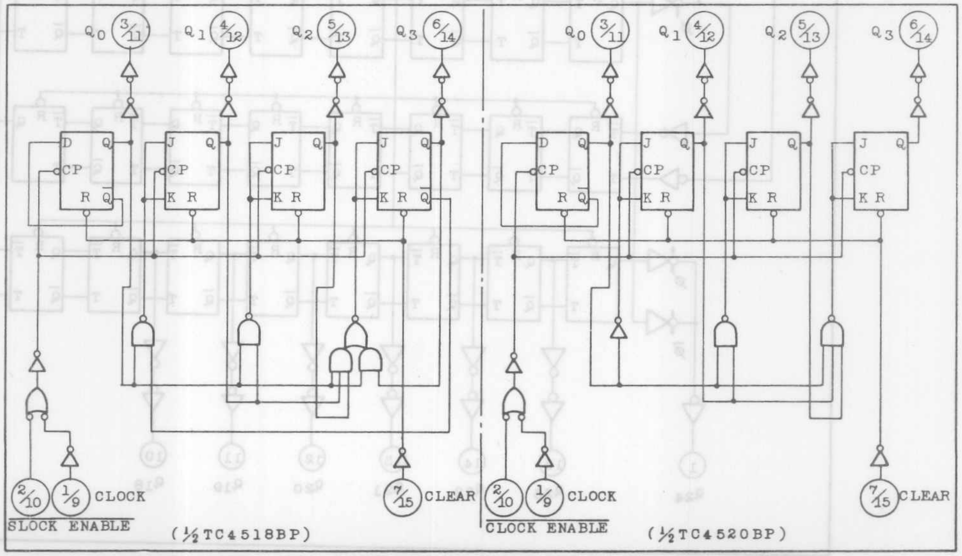


Fig. 2-160 TC4518BP DUAL BCD UP COUNTER
TC4520BP DUAL BINARY UP COUNTER

TC4518BP and TC4520BP shown in Fig. 2-160 contain 2 circuits of BCD up-counter and 4-bit binary up-counter, and are advantageous in counting BCD 2 digits on more, or binary 5-bits or more.

TC40160BP ~ TC40163BP are presettable 4-bit counters that have cascade connection function. Pin connections and functions of these counters are same as those of 74160 ~ 74163 TTL. Preset operations are all synchronized with a clock, and these counters can be classified into clock synchronous type (TC40162BP/TC40163BP) and asynchronous type (TC40160BP/TC40161BP).

TC40160BP and TC40162BP are BCD counters, and TC40161BP and TC40163 BP are 4-bit binary counters.

TC4510BP, TC4516BP and TC4029BP are presettable up/down 4-bit counters. TC4510BP is of BCD type and TC4516BP is of 4-bit binary type. TC4029BP can be used either for BCD/binary counting by the BCD/BINARY switching terminal. TC4510BP and TC4516BP have clear input, while TC4029BP is not provided with it.

Therefore, to clear TC4029BP, it is necessary to preset "0". With all of these 3 types, clear and preset (load) inputs are of asynchronous type. The logic diagram of TC4029BP is shown in Fig. 2-161.

TC4017BP is a decimal counter based on the 5-bit Johnson counter and 10 decode outputs can be obtained, which are useful for control circuits as no hazard appears in the circuits. TC4022BP is an octal counter in the same format.

A decimal counter may be used in one digit only, but in general it is used in many cases with several digits connected in series to make the maximum count value larger.

For application of these, 4-digit and 6-digit LSI decimal counters are available for C^2MOS.

TC5001P, TC5037P, TC5051P and TC5052P are 4-digit decimal up-counters. Each digit synchronizing with inner clock (scanner) are outputed with the time sharing.

TC5010P is a 4-digit decimal counter of which all outputs are static and obtained at 16 terminals.

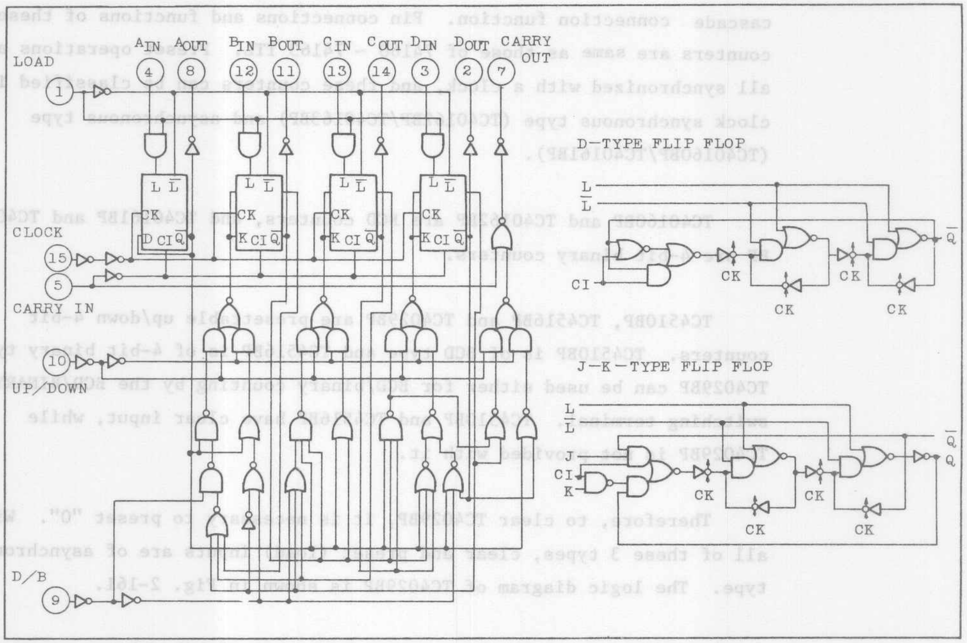


Fig. 2-161 TC4029BP PRESETTABLE 4 BIT UP/DOWN COUNTER

TC5032P is a 6-digit decimal counter capable of high-speed initial stage counting, and its output is of 6-digit dynamic format.

These counters can be broadly used in various systems such as total counter, frequency counter, A/D converter, etc.

The block diagram of TC5032P is shown in Fig. 2-162.

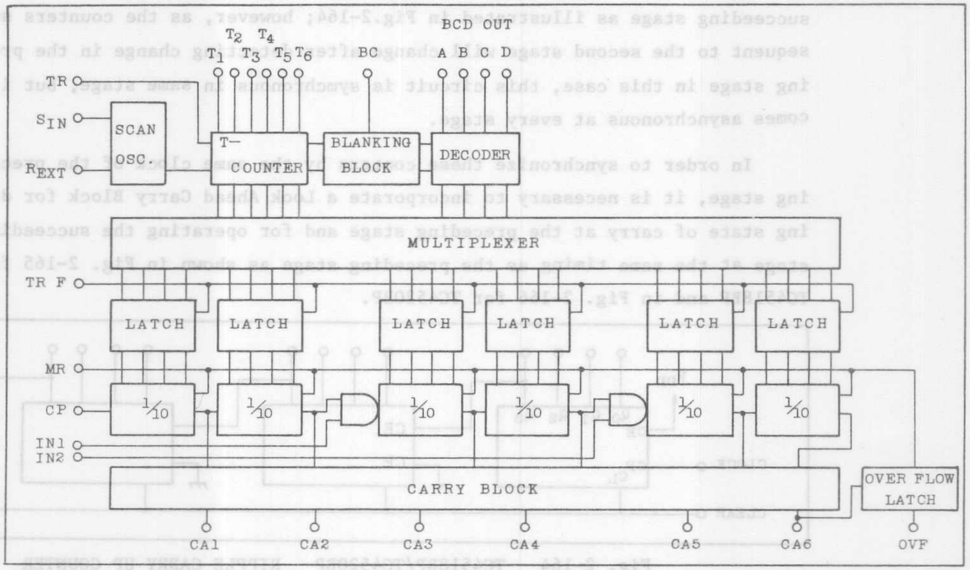


Fig. 2-162 TC5032P 6 DIGIT DECODE COUNTER

5.3 Application of counter IC

(1) Cascade connection of counter IC

When pulse counting/division is performed using one counter IC, it may not be practical in many cases to use only one counter IC being provided with one digit as TC4020BP etc. For this reason, a techenique of cascade connection of counter ICs is generally used.

Shown in Fig. 2-163 is an example of the cascade connection of ripple carry binary counters, and number of stages can be increased easily by connecting arbitrary outputs to clock inputs at succeeding stages.

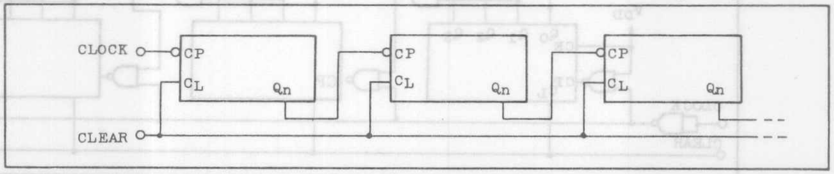


Fig. 2-163 Cascade Connection of TC4020BP (TC4040BP, TC4024BP)

To connect TC4518BP and TC4520BP counters that contain 2 circuits, Q_3 output at the preceding stage is to be connected to the enable input at the succeeding stage as illustrated in Fig.2-164; however, as the counters subsequent to the second stage will change after detecting change in the preceding stage in this case, this circuit is symchronous in same stage, but it becomes asynchronous at every stage.

In order to synchronize these conters by the same clock of the preceding stage, it is necessary to incorporate a Look Ahead Carry Block for detecting state of carry at the preceding stage and for operating the succeeding stage at the same timing as the preceding stage as shown in Fig. 2-165 for TC4518BP and in Fig. 2-166 for TC4520BP.

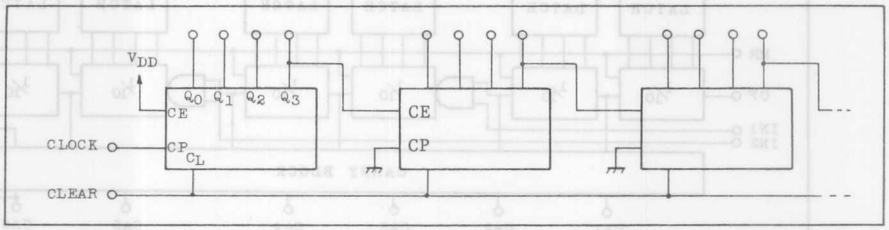


Fig. 2-164 TC4518BP/TC4520BP RIPPLE CARRY UP COUNTER

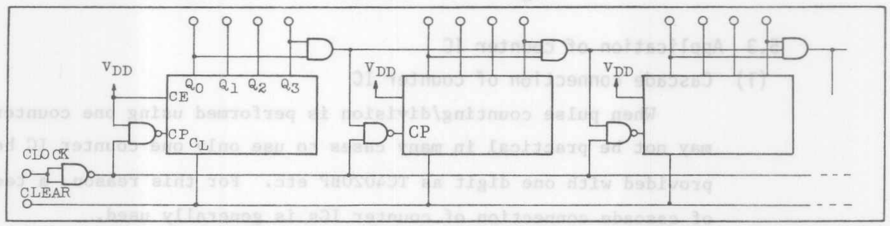


Fig. 2-165 TC4518BP PARALLEL CARRY UP COUNTER

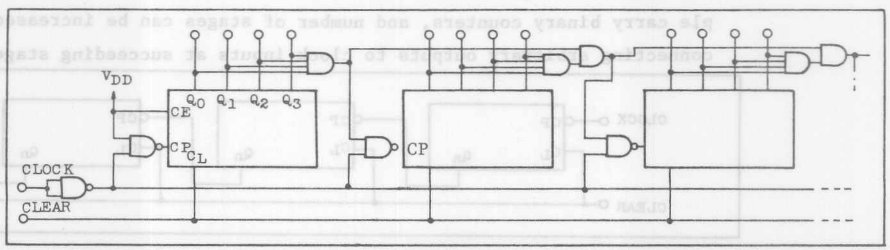
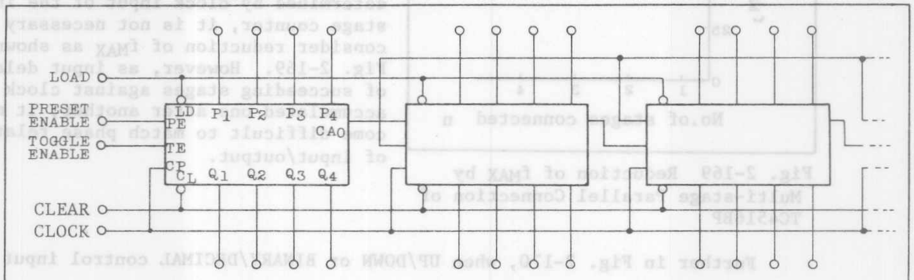


Fig. 2-166 TC4520BP PARALLEL CARRY UP COUNTER

The presettable counters (TC40160BP ~ TC40163BP, TC4510BP, TC4516BP and TC4029BP) have the look ahead carry block built in IC, and it is therefore possible to structure a full digit synchronous counter simply by connecting carry input/output.

Fig. 2-167 shows a parallel carry counter with TC40160BP ~ TC40163BP cascade-connected.



PE	TE	FUNCTION
H	H	Count
L	*	No Count
*	L	No Count

Fig. 2-167 TC40160BP/161BP/162BP/163BP PARALLEL CARRY COUNTER

Fig. 2-168 shows a parallel carry up/down counter of cascade-connected TC4029BP (TC4510BP, TC4516BP). With these counters having the lood ahead carry block, a counter at the succeeding stage is operated by carry information given by the preceding stage; therefore, the more the stages are connected, the larger cumulative carry transmission time becomes, and max. system operating frequency is reduced.

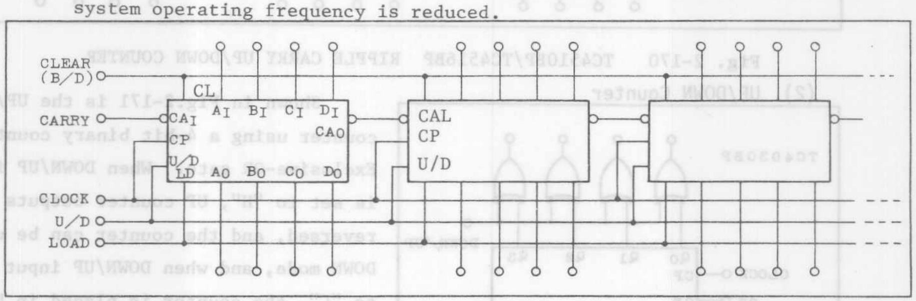


Fig. 2-168 TC4029BP/TC4510BP /TC4516BP PARALLEL CARRY UP/DOWN COUNTER

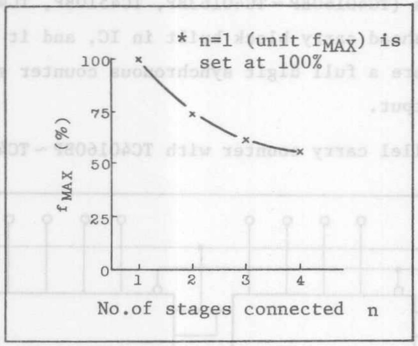


Fig. 2-169 Reduction of f_{MAX} by Multi-stage Parallel Connection of TC4516BP

Shown in Fig. 2-169 is max. operating frequency reduction effect in a n-stage parallel carry connecting circuit that uses TC4516BP. As a matter of cource, it is possible to constitute an asynchronous counter shown in Fgi. 2-170 by connecting carry outputs from these counters to the succeeding stage clock inputs. In this case, as system response speed $f_{(MAX)}$ is determined by clock input of the initial stage counter, it is not necessary to consider reduction of f_{MAX} as shown in Fig. 2-169. However, as input delay time of succeeding stages against clock are accumulated one after another, it may become difficult to match phase relations of input/output.

Further in Fig. 2-170, when UP/DOWN or BINARY/DECIMAL control input is changed during operation, CARRY output may change depending upon count mode and advance count at the succeeding stage by one; therefore, timing for switching must be carefully selected.

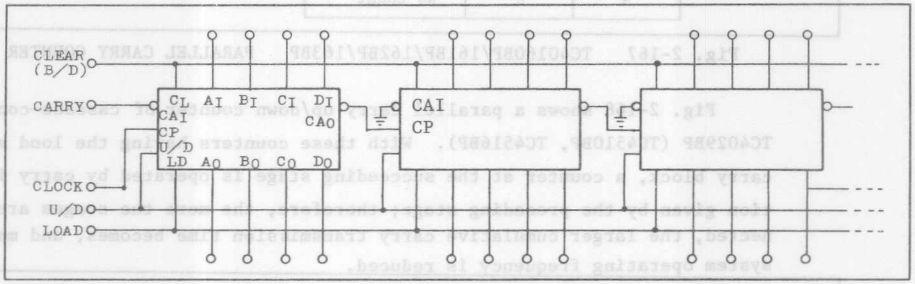


Fig. 2-170 TC4510BP/TC4516BP RIPPLE CARRY UP/DOWN COUNTER

(2) UP/DOWN Counter

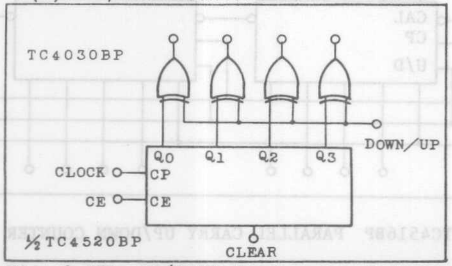


Fig. 2-171 UP/DOWN Counter Consisting of UP Counter and Ex-OR Gate

Shown in Fig.2-171 is the UP/DOWN counter using a 4-bit binary counter and Exclusive-OR gate. When DOWN/UP input is set to "H", UP counter outputs are all reversed, and the counter can be used in DOWN mode, and when DOWN/UP input is set to "L", the counter is placed in UP mode.

Fig. 2-172 shows the reversible UP/DOWN counter using TC4510BP and R/S flip-flop.

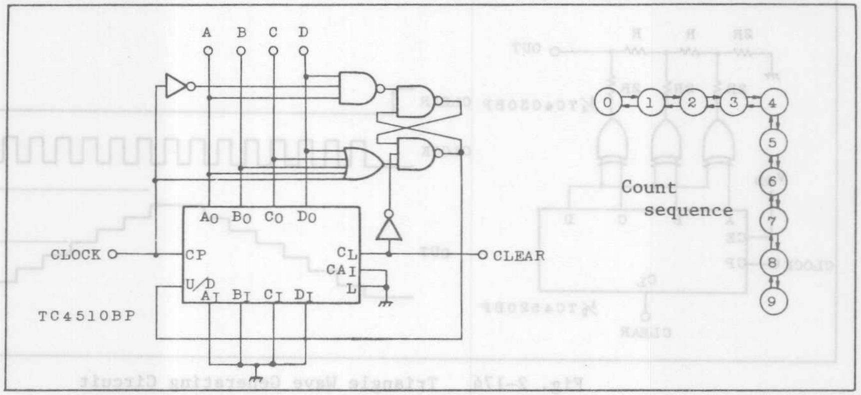


Fig. 2-172 Reversible UP/DOWN Counter (I)

As shown in Fig.2-172, when counting is started from "0" and count content becomes "9", the counter is automatically shifted to DOWN·mode and counts down to "0".

That is, UP mode and DOWN mode are automatically switched alternately. If "0" detection and "9" detection gates are changed to other number counter detection gates, the counter can be made to a reversible counter that reverses under optional counting state. Further, if it is desirable to start counting from optional state,set the initial state using LOAD terminal of TC4510BP.

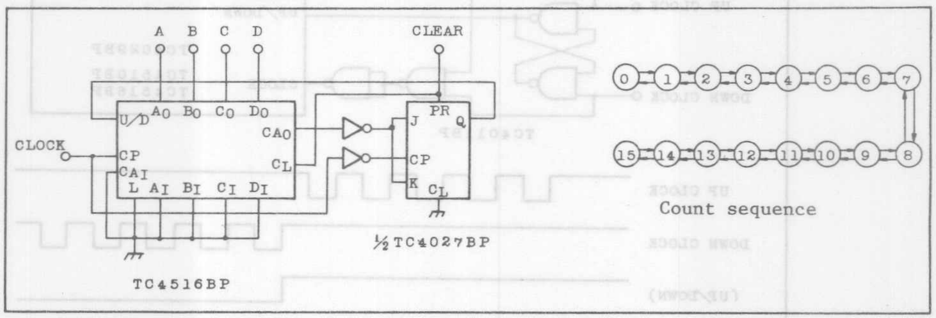


Fig. 2-173 Reversible UP/DOWN Counter (II)

Fig. 2-173 shows a reversible UP/DOWN counter that switches UP and DOWN modes by detecting carry of the UP/DOWN counter.

In this diagram, if TC4516BP is changed to TC4510BP, the counter becomes the one that performs counting similar to that shown in Fig. 2-173.

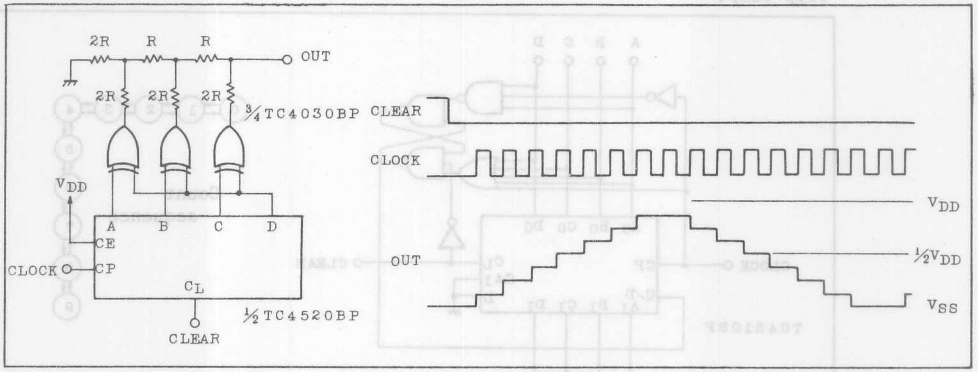


Fig. 2-174 Triangle Wave Generating Circuit

Fig.2-174 shows a reversible UP counter with the UP counter shown in Fig. 2-171 applied.

When a R-2R rudder network is connected to the output, a triangle wave generating circuit that provides 8-stage analog output according to clock input can be structured. In this case, however, it is necessary to set R at a sufficiently large value comparing with output impedance of CMOS ($R \geqq$ several 10kΩ).

TC4510BP/TC4516BP/TC4029BP are in a form of selecting UP count and DOWN count using UP/DOWN switching input.

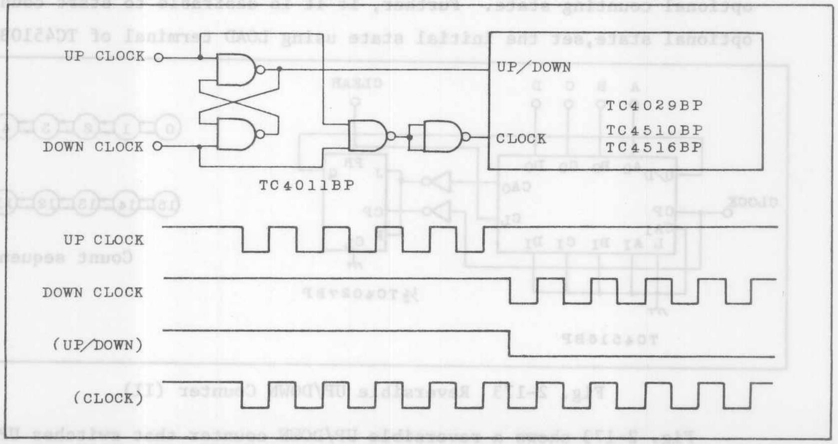


Fig. 2-175 UP/DOWN Separate Clock Counter

However, it may be necessary in many cases to provide 2 clock input lines; UP clock and DOWN clock input lines for selecting UP and DOWN clocks.

The UP/DOWN selecting circuit as shown in Fig. 2-175 is available for such applicaiton.

On this counter, when one of the clocks is being given, another clock must be placed at "H". If it is at "L", the clock will be inhibited.

(3) Programmable 1/N divider

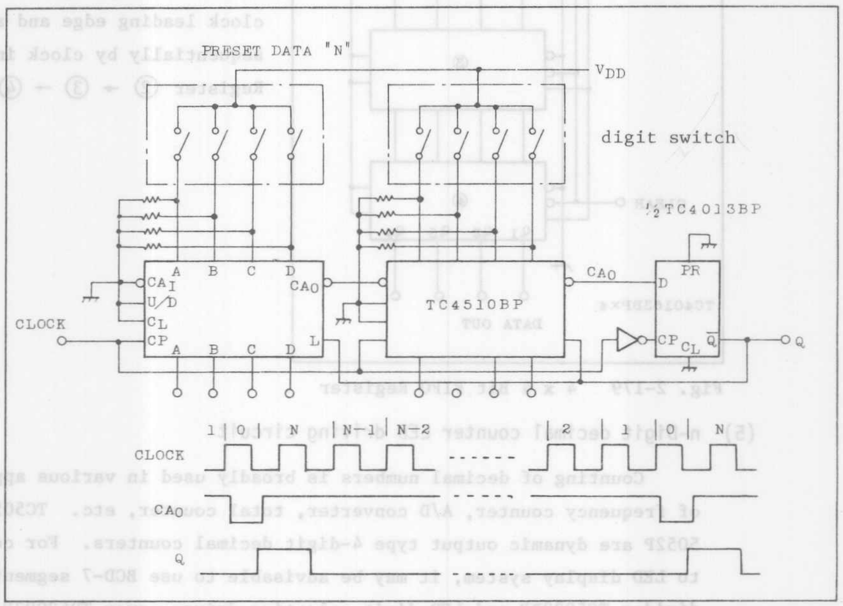


Fig. 2-176 Programmable 1/N+1 Divider

Shown in Fig.2-176 is a programmable divider using TC4510BP. By pre-setting "N" with a digit switch, 1/N+1 clock frequency can be obtained at output Q.

TC4018BP is 1/N programmable divider based on the 5-bit Johnson counter, and arbitrary division 1/2 ~1/9 is possible as illustrated in Fig. 2-177.

(4) 4x4 Bit FIFO register

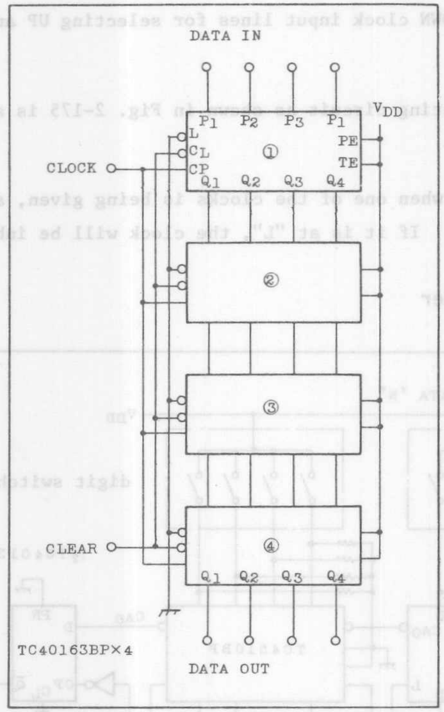


Fig. 2-179 4 x 4 Bit FIFO Register

TC40161BP and TC40163BP are 4-bit UP counters having SYNCHRONOUS PRESET function. As these counters read parallel data at clock leading edge, a 4-bit x 4 FLFO Register can be structured when n-units of the counters are, in parallel, used as shown in Fig. 2-179. 4-bit input given to DATA IN is taken by Register ① at clock leading edge and shifted sequentially by clock in order of Register ② → ③ → ④.

(5) n-Digit decimal counter LED driving circuit

Counting of decimal numbers is broadly used in various applications of frequency counter, A/D converter, total counter, etc. TC5051P and TC 5052P are dynamic output type 4-digit decimal counters. For converting to LED display system, it may be advisable to use BCD-7 segment decoder/ divider TC5022BP and LED digit selecting driver array TD62003P.

Fig.2-181 shows an example of similar system configured by using 6 digit decimal counters.

Counting up to 9999 is possible in the circuit shown in Fig. 2-180 and max. 999999 in the circuit in Fig. 2-181.

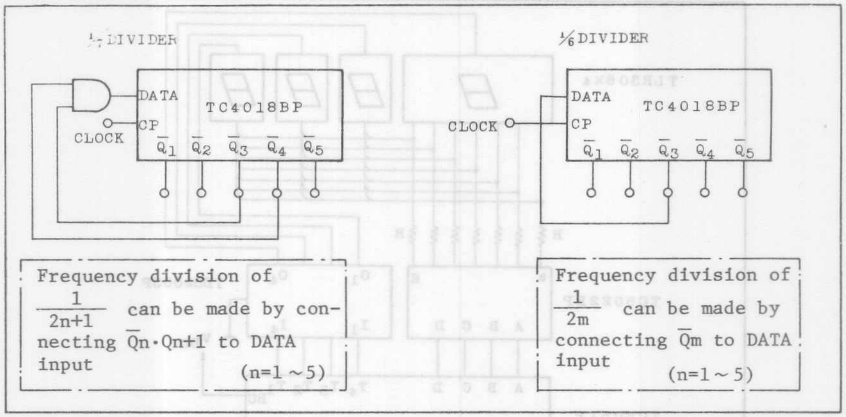


Fig. 2-177 1/N Divider Using TC4018BP

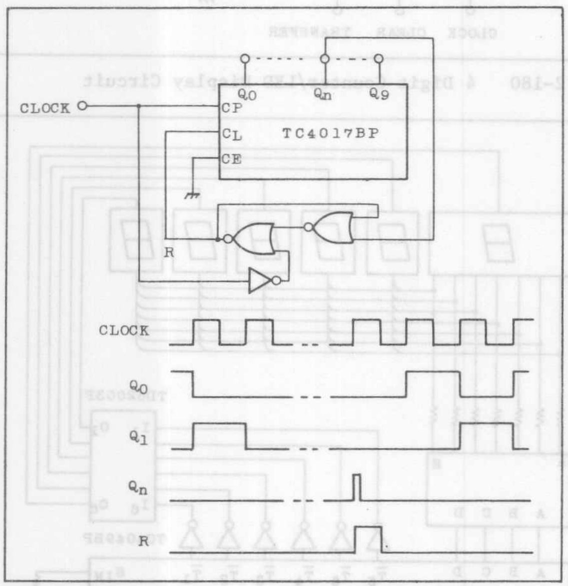


Fig. 2-178 Programmable 1/N divider

When output from TC 4017BP (or TC4022BP) is connected to CLEAR input through R/S flip-flop as shown in Fig. 2-178, a programmable divider can be composed.

A method to connect output Q directly to CLEAR is often used; however, CLEAR pulse width becomes extremely short and operation can possibly become unstable. Therefore, this is not preferable.

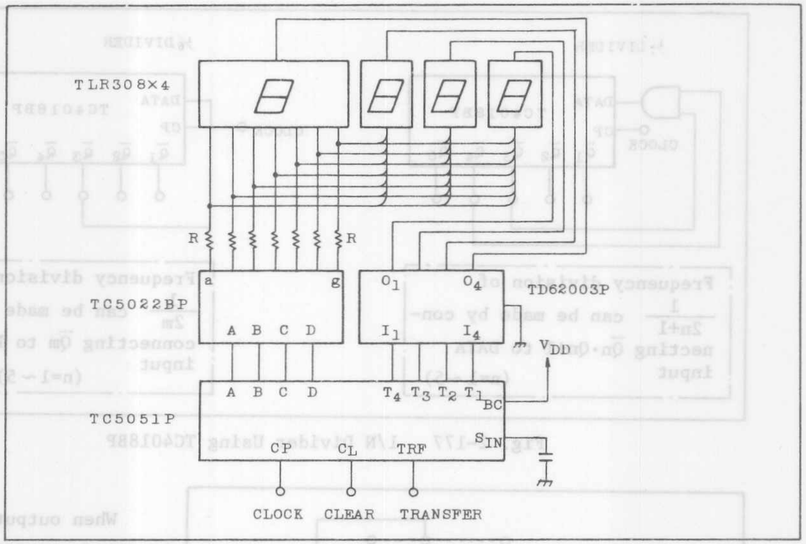


Fig. 2-180 4 Digit Counter/LED Display Circuit

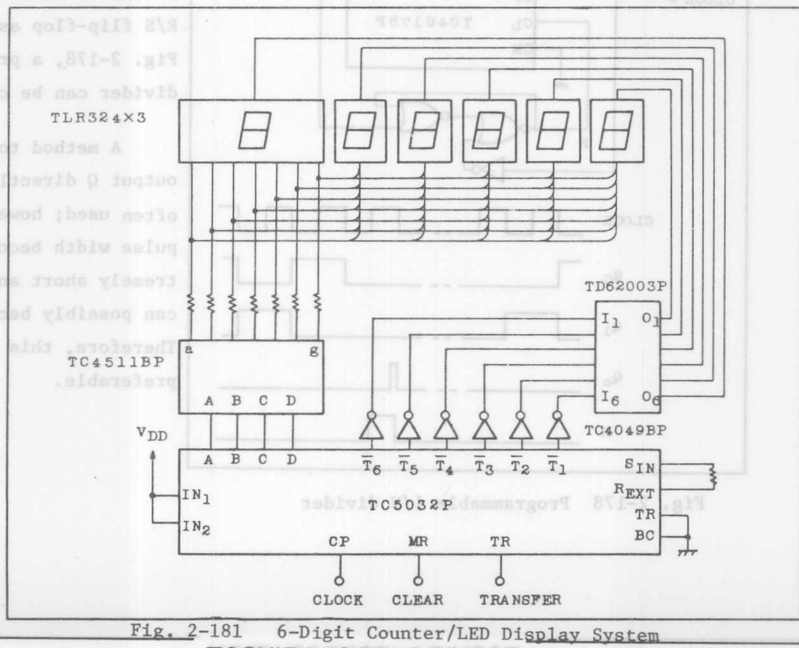


Fig. 2-181 6-Digit Counter/LED Display System

(6) Binary-BCD code conversion circuit (BCD - Binary)

Using presettable binary DOWN counters and BCD UP counters, a binary to BCD code conversion circuit can be configured.

An example of its fundamental circuit is shown in Fig.2-182. When SW is turned on, binary data input is loaded to the binary counters and BCD counters are cleared to "0". When SW is turned off, the oscillation circuit is activated and both the binary counter and BCD counter start counting simultaneously. If clock is stopped when state of the binary counter under DOWN mode becomes "0", count value of BCD UP counter at that time is converted to BCD output.

This type of code converter has more BCD input/output lines than input binary lines. That is, when binary input is 12 bits and converted to decimal number, $2^{12}=4096$. Therefore, counting capacity up to 4095 becomes necessary and it is required to prepare BCD counters for 4 digits. Further, the conversion time is indicated by $4096 \cdot T$ where T is the oscillation period of the oscillator. In Fig.2-182, as $T \fallingdotseq 5$ μs, $5\times10^{-6}\times4096 \fallingdotseq 20\times10^{-3}$ (20 ms) is required.

Code conversion of BCD to binary is possible when the presettable DOWN counter shown in Fig. 2-182 is substituted with a BCD counter (TC4510BP) and UP counter with a binary counter (TC4520BP).

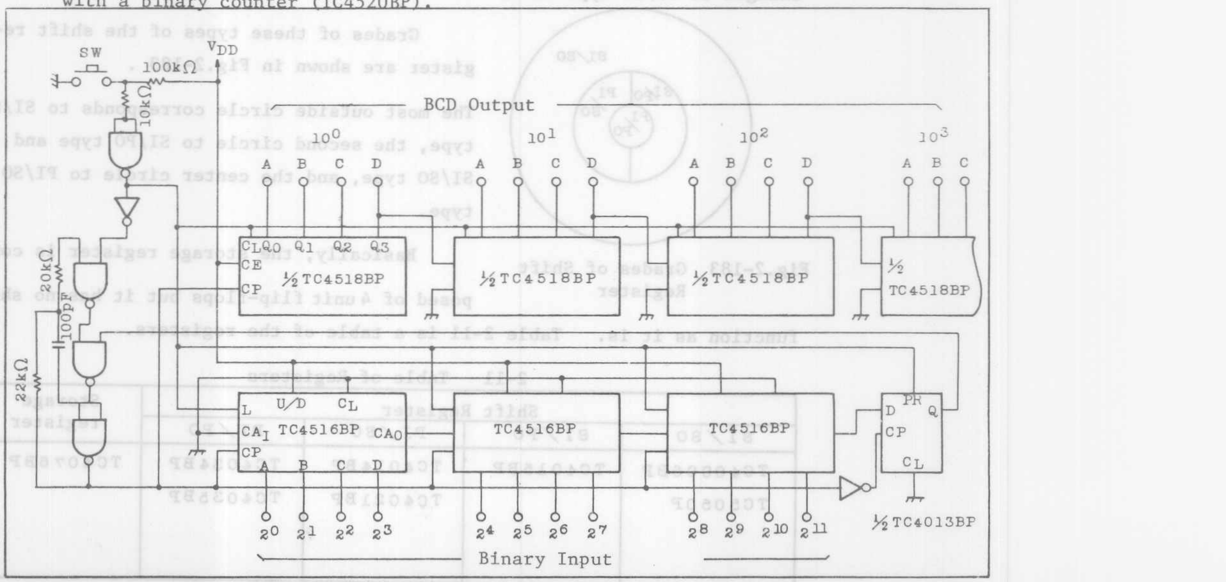


Fig. 2-182 Binary - BCD Conversion Circuit

6. Register

In a broader sense, a register is a memory temporarily storing data. Registers of C^2MOS are classified into a shift register and a storage register. The shift register is used for serial/parallel conversion and storage of data. The storage register, as implicated by its name, is used for data storage.

6.1 Types of register

The shift register is classified into following 4 types according to input/output methods of data:

i) Serial In - Serial Out

ii) Serial In - Parallel Out

iii) Parallel In - Serial Out

iv) Parallel In - Parallel Out

Each of these types of the shift register is not a fixed type but can be converted to other types depending upon circuit configuration.

That is, PI/PO type in iv) can be changed to any type in i) ~ iii) by changing connection. SI/PO type in ii) and PI/SO type in iii) can be changed to SI/SO type in i).

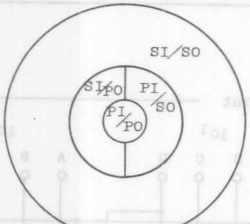


Fig.2-183 Grades of Shift Register

Grades of these types of the shift register are shown in Fig.2-183 .

The most outside circle corresponds to SI/SO type, the second circle to SI/PO type and SI/SO type, and the center circle to PI/SO type.

Basically, the storage register is composed of 4 unit flip-flops but it has no shift function as it is. Table 2-11 is a table of the registers.

2-11 Table of Registers

Shift Register				Storage register
SI/SO	SI/PO	PI/SO	PI/PO	
TC40006BP	TC4015BP	TC4014BP	TC4034BP	TC4076BP
TC5050P		TC4021BP	TC4035BP	

(1) Serial input shift register

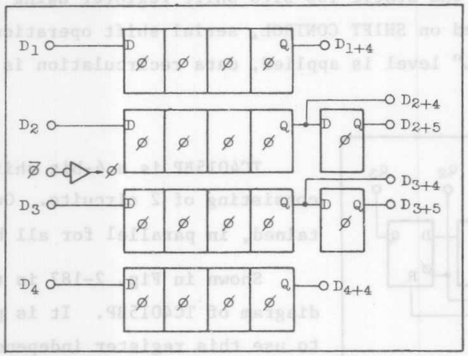


Fig.2-184 TC4006BP 18 Bit Static Shift Register

TC4006BP is a shift register consisting of 18 flip-flops commonly using same clock, and two circuits of 4-bit register and 5-bit register have been inserted, respectively. Depending upon connecting methods, this register can be used as a min. 4-bit or max. 18-bit register

Fig.2-184 shows the block diagram of TC4006BP.

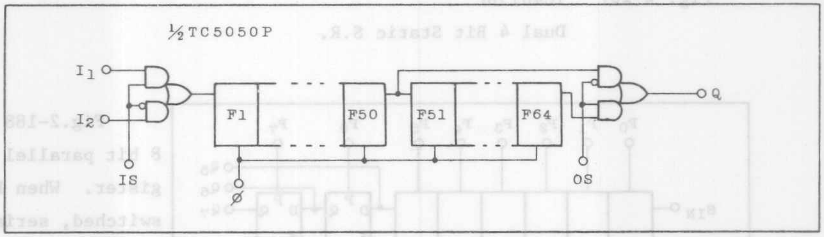


Fig. 2-185 TC5050P Dual 50/64 Bit Static S.R.

Fig. 2-185 shows the dual 50/64 bits static shift register TC5050P. As either one of data input I_1 or I_2 can be selected by input IS, data recirculation is easy. Furthermore, it is also possible to select 50 bits and 64 bits by input OS. In addition, as two circuits are incorporated in one package, it is possible to configurate 50, 64, 100, 114 and 128 bits.

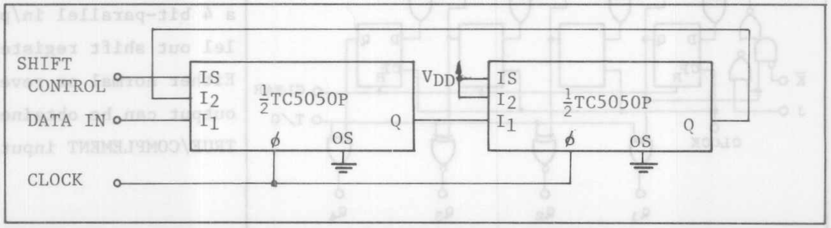


Fig. 2-186 100 Bit Static Shift Register

Fig. 2-186 shows the static 100 bits shift register using TC5050P. If "H" level is applied on SHIFT CONTROL, serial shift operation is achievable. And if "L" level is applied, data recirculation is achievable.

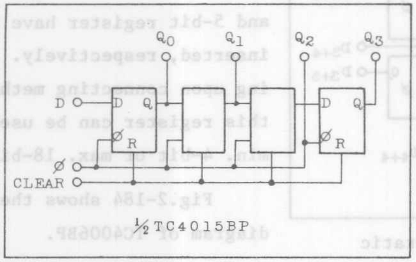


Fig. 2-187 TC4015BP

Dual 4 Bit Static S.R.

TC4015BP is a 4-bit shift register consisting of 2 circuits. Output is obtained, in parallel for all bits.

Shown in Fig. 2-187 is the logic diagram of TC4015BP. It is possible to use this register independently for 4 bits or 8 bits.

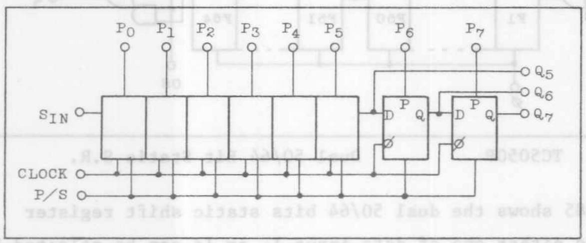


Fig. 2-188 TC4014BP TC4021BP 8 Bit Static S.R.

Fig.2-188 shows the 8 bit parallel shift register. When P/S input is switched, serial input S_{IN} becomes enables.

TC4014BP is of synchronous parallel input type, while TC4021BP is of asynchronous parallel input type.

Shown in Fig.2-188 is a 4 bit-parallel in/parallel out shift register. Either normal or reversed output can be obtained by TRUE/COMPLEMENT input.

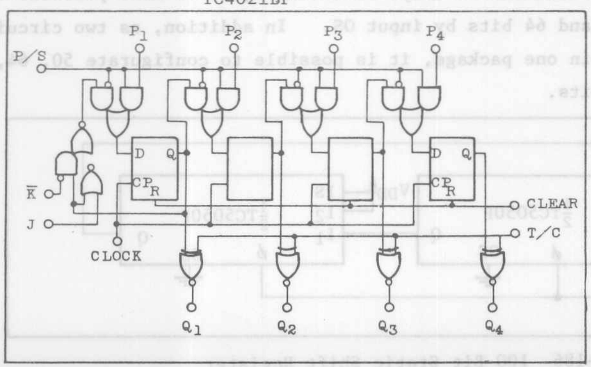


Fig. 2-189 TC4035BP 4 Bit Static S.R.

TC4034BP is a 8 bit-shift register having 2 channels of 8-bit parallel data bus. Eight signal lines $A_0 \sim A_7$ and $B_0 \sim B_7$ can be used as either parallel input or parallel output. Since these data buses have 3-state function, they can be connected direct to bus line of a microcomputer.

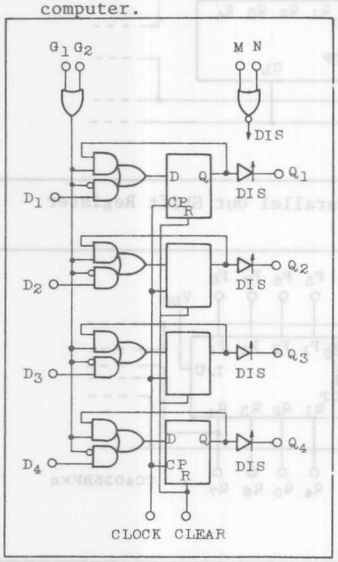


Fig. 2-190 TC4076BP
4 Bit Storage Register

TC4076BP shown in Fig. 2-190 is a 4-bit storage register. When both of Input Disable input G_1 and G_2 are at "L" level, each F/F takes in data at the leading edge of clock.

Output becomes enable when both of Output Disable M and N are at "L" level, and if either one is at "H" level outputs become high impedance.

6.2 Application of register

(1) Basic connection of shift register

A shift register can be expanded simply by connecting the final stage data output to the initial data input of succeeding IC, and number of bits can be easily expanded. Fig. 2-191 is a serial in and parallel out shift register consisting of cascade-connected TC4015BP. Fig. 2-192 and Fig. 2-193 show N bit parallel in/parallel out shift register consisting of cascade-connected TC4035BP and TC4034BP, respectively.

As a matter of course, shift mode is synchronized with clock; however, parallel input may be synchronous or asynchronous with clock. In the example using TC4035BP shown in Fig. 2-192, parallel input is synchronized with clock at its leading edge.

In Fig. 2-193, A/S input is asynchronous when it is at "H" level, while it is synchronized with clock at "L" level.

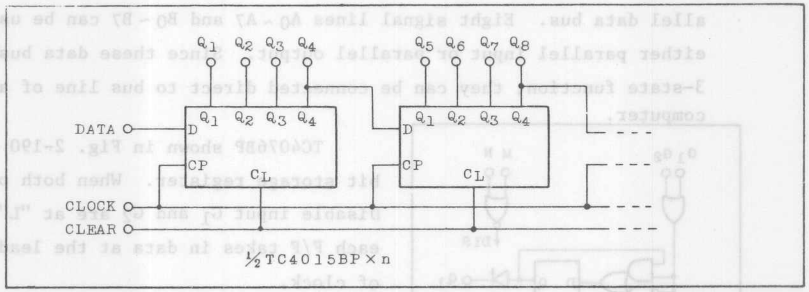


Fig.2-191　N-Bit Serial In/Parallel Out Shift Register

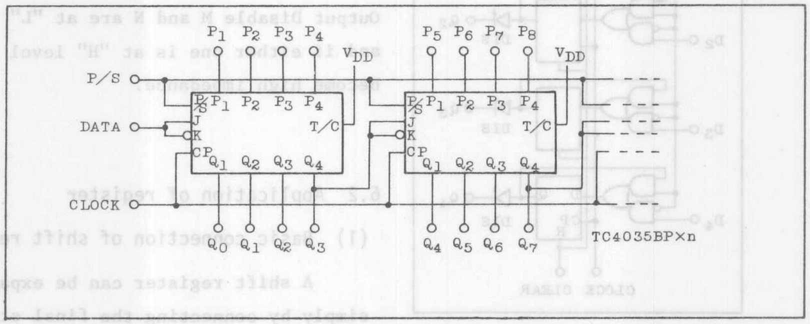


Fig.2-192　N-Bit Parallel In/Serial Out Shift Register

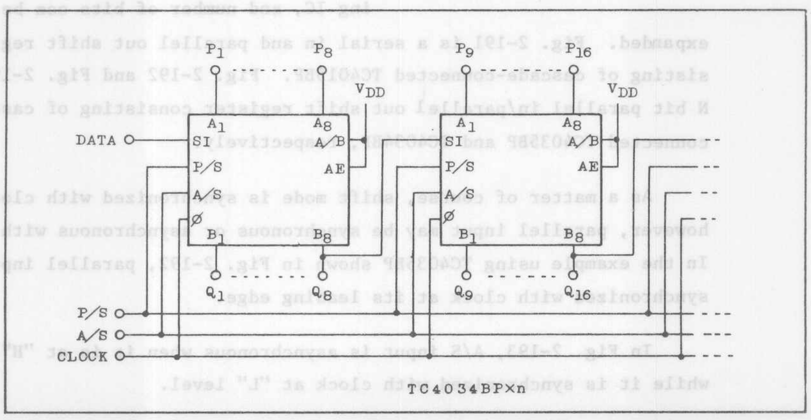


Fig.2-193　N-Bit Parallel In/Parrallel Out Shift Register

(2) Data serial/parallel conversion circuit

When the serial in/parallel out shift register TC4015BP and the 2-circuit, 4-bit ratch TC4508BP are used, it is possible to make parallel conversion of 8-bit serial data. Shown in Fig.2-194 is an example of this connection. In this diagram, direct connection with a 8-bit bus line is possible using DISABLE input of TC4508BP.

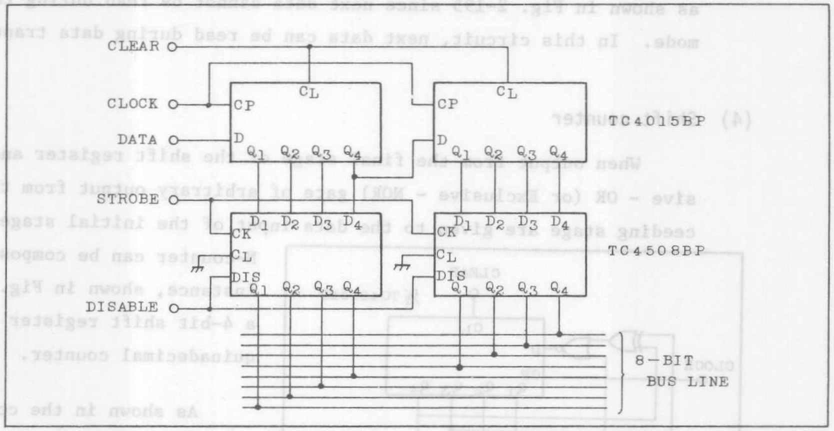


Fig. 2-194 Serial/Parallel Conversion Circuit

(3) Data parallel/serial conversion circuit

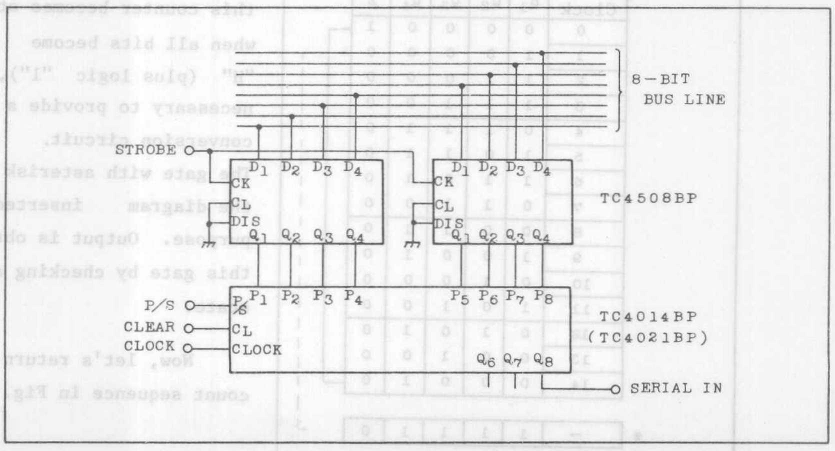


Fig. 2-195 Parallel/Serial Conversion Circuit

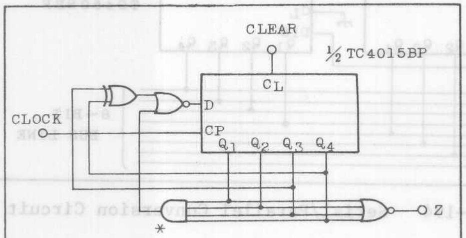
For parallel/serial conversion of data, a system for sequential data output with the address counter using a multiplexer is described in the foregoing; however, in this case, a 8-bit parallel in/serial out register is generally used. Although one register in a circuit may be sufficient, input may be given through a buffer register in many cases as shown in Fig. 2-195 since next data cannot be read during the shift mode. In this circuit, next data can be read during data transmission.

(4) Shift counter

When output from the final stage of the shift register and Exclusive - OR (or Exclusive - NOR) gate of arbitrary output from the succeeding stage are given to the data input of the initial stage, N-counter can be composed. For instance, shown in Fig. 2-196 is a 4-bit shift register based quinadecimal counter.

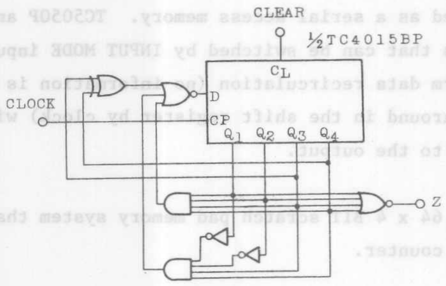
As shown in the count sequence in this diagram, the count returns to the original mode after 15 clocks. However, since this counter becomes static when all bits become "H" (plus logic "1"), it is necessary to provide a forced conversion circuit.
The gate with asterisk (*) in the diagram inserted for this purpose. Output is obtained at this gate by checking arbitrary state.

Now, let's return to the count sequence in Fig. 2-196.

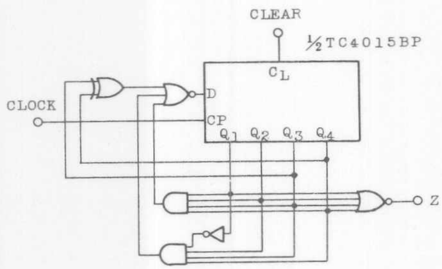


Clock	Q_1	Q_2	Q_3	Q_4	Z
0	0	0	0	0	1
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	0	1	1	1	0
5	1	0	1	1	0
6	1	1	0	1	0
7	0	1	1	0	0
8	0	0	1	1	0
9	1	0	0	1	0
10	0	1	0	0	0
11	1	0	1	0	0
12	0	1	0	1	0
13	0	0	1	0	0
14	0	0	0	1	0
* –	1	1	1	1	0

Fig.2-196 Shift Counter (Quinadecimal Divider)



Decimal shift counter



Duodecimal shift counter

Fig. 2-197 Shift Counter (N-counter)

Under the state shown, the counter only repeats the 1/15 division. If the initial stage bit is forced to invert when the counter is shifted from arbitrary state to next state, jump in the loop becomes possible. For instance, the counter is shifted from "0000" to "0011" mode in sequence by the 8th clock, and by next one clock input to "1001" mode. If the shift register input is turned to "0", it is placed in "0001" mode by the 9th clock. As this "0001" mode is equivalent to the 14th clock of the loop, it is returned to "0000" by next clock. That is, as the counter is shifted to the 14th clock from the 8th clock jumping 5 modes of 9, 10, 11, 12 and 13th clock, it performs the decimal operation.

Shown in Fig. 2-197 are a decimal shift counter and a duodecimal shift counter with this jump gate added. By changing this jump gate, various divisions become possible.

In general, shift counters up to 2^n can be composed using n-bit shift register. However, if number of bits is increased, the loop is divided into several loops, and it may be therefore necessary to provide an escape pass from an unused loop. Further, as the loop is divided, number of count become equal to or less than 2^n.

(5) Scratch pad memory

A mass storage shift register itself stores much informations and therefore, it can be used as a serial access memory. TC5050P and TC 5004P have 2 data inputs that can be switched by INPUT MODE input and it is possible to perform data recirculation (no information is lost as same data is turned around in the shift register by clock) with one of the inputs connected to the output.

Fig. 2-198 shows a 64 x 4 BIT scratch pad memory system that uses TC4516BP as the address counter.

Access time is expressed by max. 64T where T is the clock cycle.

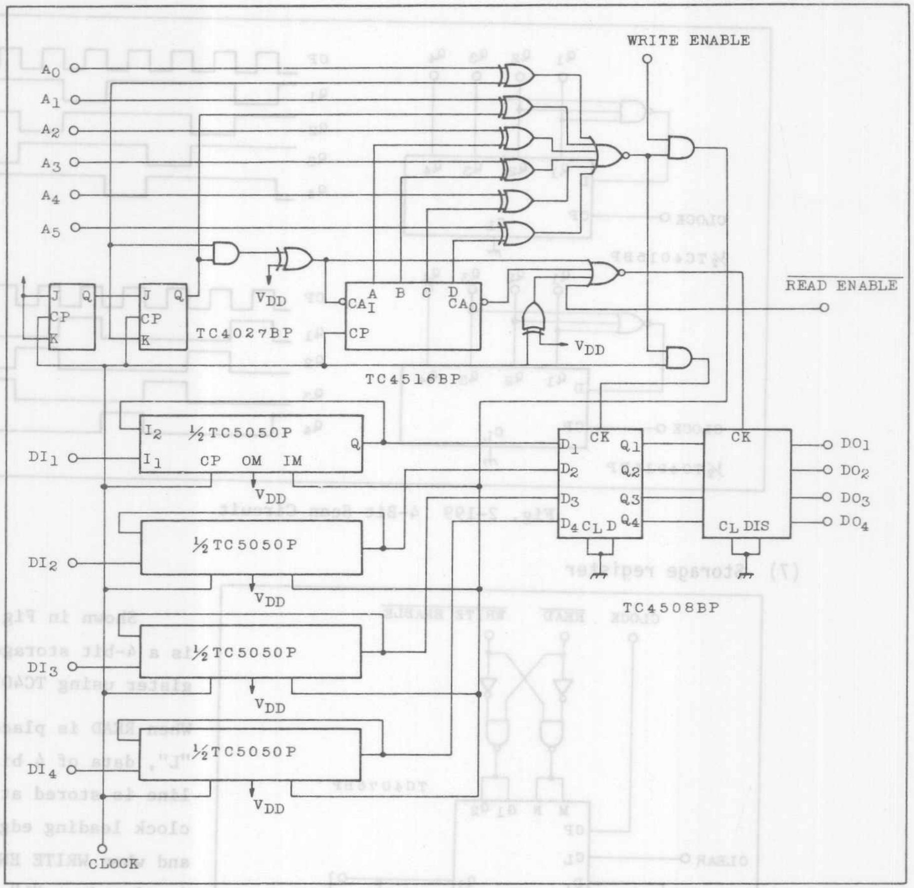


Fig. 2-198 Scratch Pad Memory System (64 x 4 bits)

(6) Scan circuit

When n-bit shift register is structured using TC4015BP and NAND of all outputs from the initial stage to n-1 bit or NOR gate output is connected to the initial stage D input, a n-bit scan counter can be structured.

Fig. 2-199 shows an example of 4-bit scan circuit.

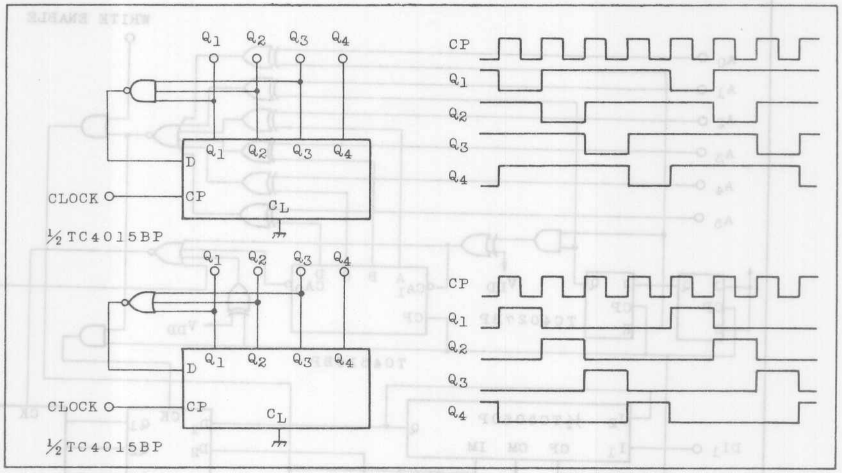


Fig. 2-199 4-Bit Scan Circuit

(7) Storage register

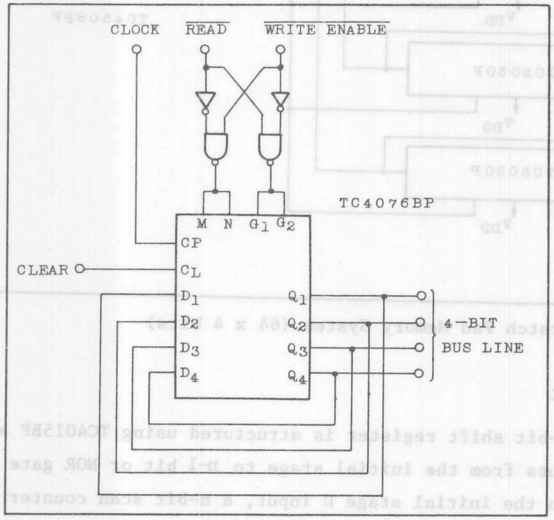


Fig. 2-200 4-Bit Storage Register

Shown in Fig. 2-200 is a 4-bit storage register using TC4076BP.

When $\overline{\text{READ}}$ is placed at "L", data of 4 bit bus line is stored at the clock leading edge, and when $\overline{\text{WRITE ENABLE}}$ is placed at "L", the storage content is output to the bus line.

7. Arithmetic Circuit

The arithmetic circuit is normally a logic circuit that performs arithmetic operation, and the most representative one is an adder. Both binary and BCD adders are available for C^2MOS. Since subtraction can be achieved by adding complements from its algarism, no subtraction circuit is made available.

There are various methods proposed for addtion, subtraction, etc. Recently, there arithmetic operations are generally processed using a microcomputer, etc. rather than using a combination of many ICs. In this section, the basic arithmetic circuit is introduced and comparator IC and others are explained.

7.1 Types of arithmetic circuit

Table 2-12 Table of Arithmetic Circuits

Function		Product Name
Adder	Binary serial	TC4032BP TC4038BP
	Binary 4-bit parallel BCD parallel	TC4008BP TC4560BP
Complementer	Complementer of "9"	TC4561BP
Parity tree	12 bits	TC4531BP
Multiplier	BCD rate	TC4527BP
Magnitude Comparator	4 bits	TC4063BP TC4585BP

Table 2-12 is a table of the arithmetic circuits.

(1) Adder

TC4032BP and TC4038BP are 3-circuit binary serial adder. As both of input and output are serially processed, it is normally required to store added results with a n-bit shift register connected to the output.

TC4008BP is a 4-bit binary parallel adder.

The sums of 4-data inputs $A_1 \sim A_4$ and 4 data inputs $B_1 \sim B_4$ are output at $S_1 \sim S_4$ and CARRY OUT. As Look Ahead Carry system is employed for CARRY OUT, carry is performed quickly in case of cascade connection.

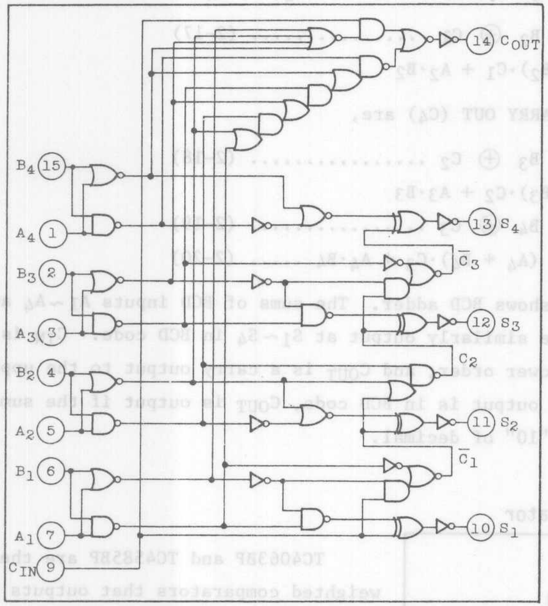


Fig. 2-201 TC4008BP 4 Bit Full Adder

Fig. 2-201 shows the logic diagram of TC4008BP.

In this diagram, a total sum of CARRY IN from the lower order and the least significant bit input A1, and A_2 is obtained at the adding output S_1 and internal carry signal to upper order.

(C_1)

The logical expression of S_1 is expressed by

$S_1 = A_1 \oplus B_1 \oplus C_{IN}$ ...(2-16)

The logical expression of C_1 is expressed by

$C_1 = (A_1 + B_1) \cdot C_{IN} + A_1 \cdot B_1$

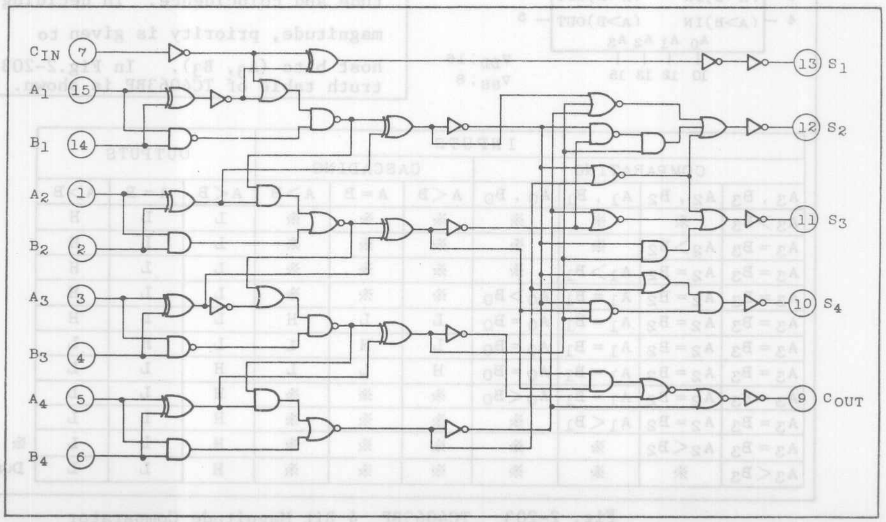


Fig. 2-202 TC4560BP BCD Adder

Similarly, the logical expressions of S_2 and C_2 are as follow;

$$S_2 = A_2 \oplus B_2 \oplus C_1 \quad \text{..............} \quad (2\text{-}17)$$

$$C_2 = (A_2 + B_2)\cdot C_1 + A_2\cdot B_2$$

S_3, C_3, S_4 and CARRY OUT (C_4) are,

$$S_3 = A_3 \oplus B_3 \oplus C_2 \quad \text{................} \quad (2\text{-}18)$$

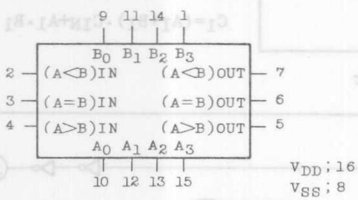
$$C_3 = (A_3 + B_3)\cdot C_2 + A_3\cdot B_3$$

$$S_4 = A_4 \oplus B_4 \oplus C_3 \quad \text{..............} \quad (2\text{-}19)$$

$$\text{CARRY OUT} = (A_4 + B_4)\cdot C_3 + A_4\cdot B_4 \quad \text{.....} \quad (2\text{-}20)$$

Fig. 2-202 shows BCD adder. The sums of BCD inputs $A_1 \sim A_4$ and BCD inputs $B_1 \sim B_4$ are similarly output at $S_1 \sim S_4$ in BCD code. C_{IN} is a carry input from the lower order, and C_{OUT} is a carry output to the upper order. In this case, as output is in BCD code, C_{OUT} is output if the sum of [A] and [B] exceeds "10" of decimal.

(2) Magnitude comparator



TC4063BP and TC4585BP are the weighted comparators that outputs 4-bit input signal after detecting its magnitude and coincidence. In deciding the magnitude, priority is given to host bits (A_3, B_3). In Fig.2-203, the truth table of TC4063BP is shown.

INPUTS							OUTPUTS		
COMPARATING				CASCADING					
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	A<B	A=B	A>B	A<B	A=B	A>B
$A_3>B_3$	※	※	※	※	※	※	L	L	H
$A_3=B_3$	$A_2>B_2$	※	※	※	※	※	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	※	※	※	※	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	※	※	※	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	※	※	※	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	※	※	※	※	H	L	L
$A_3=B_3$	$A_2<B_2$	※	※	※	※	※	H	L	L
$A_3<B_3$	※	※	※	※	※	※	H	L	L

※ Don't Care

Fig. 2-203 TC4063BP 4 Bit Magnitude Comparator

(3) Other functions

(a) Parity tree

In the course of processing such as data transmission, arbitrary bit may be reversed due to noise or defective interface, causing erroneous operaiton. If these errors occur, it may be necessary to change or suspend the system operation. Therefore, it is effective for improving reliability of the system to provide some detecting mechanism. As the most simple error detecting system, there is the even (odd) parity system. To be concrete, parity bit of 1 bit is added to data bits so that a total sum of "H" (or "L") levels of all bits becomes always to an even (or odd) number as a whole.

Received data is checked at the data receiving side to determine whether a total sum of "H" (or "L") levels of the received data is an even or odd number, and when it is same as that at the transmission side, it is decided to be normal, and if not, it is decided that there is erroneous arbitrary one bit.

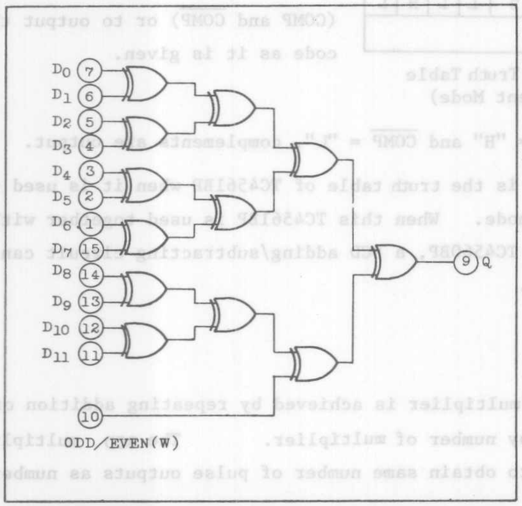


Fig. 2-204 TC4531BP 12 Bit Parity Tree

The parity tree is a circuit used for parity generation/detection, consisting of Exclusive - OR gate in a tree shape.

Fig. 2-204 shows 12-bit parity tree TC4531BP. When ODD/EVEN input is placed at "H" level, Q = "L" if a total sum of "H" levels of data inputs is an odd number, while Q = "H" if a total sum is an even number.

When ODD/EVEN input is placed at "L" level, reverse result are obtained. Therefore, the parity tree can be used for even and odd parity generation/detection.

DECIMAL INPUT CODE	ILLEGAL BCD INPUT CODE	INPUTS				DECIMAL OUTPUT CODE	OUTPUTS			
		A_4	A_3	A_2	A_1		F_4	F_3	F_2	F_1
0		L	L	L	L	9	H	L	L	H
1		L	L	L	H	8	H	L	L	L
2		L	L	H	L	7	L	H	H	L
3		L	L	H	H	6	L	H	H	L
4		L	H	L	L	5	L	H	L	H
5		L	H	L	H	4	L	H	L	H
6		L	H	H	L	3	L	L	H	H
7		L	H	H	H	2	L	L	H	L
8		H	L	L	L	1	L	L	L	H
9		H	L	L	H	0	L	L	L	L
	10	H	L	H	L	7	L	H	H	H
	11	H	L	H	H	6	L	H	H	L
	12	H	H	L	L	5	L	H	L	H
	13	H	H	L	H	4	L	H	L	L
	14	H	H	H	L	3	L	L	H	H
	15	H	H	H	H	2	L	L	H	L
※ ; Don't Care										

Table 2-13 TC4561BP Truth Table (Complement Mode)

(b) Complementer

Although it is easy to take complements in subtraction of binary number (reverse all bits), it is necessary to take complements of "9" in BCD subtraction. For producing complements of "9", some gate circuits are required. A complementer capable of outputting complements of input code "9" is available for C^2MOS.

TC4561BP is able to select either to output complements of "9" of 4-bit BCD code given by 2 control inputs (COMP and $\overline{\text{COMP}}$) or to output the input code as it is given.

When COMP = "H" and $\overline{\text{COMP}}$ = "L", complements are output.

Table 2-13 is the truth table of TC4561BP when it is used under the complement mode. When this TC4561BP is used together with the above-mentioned TC4560BP, a BCD adding/subtracting circuit can be easily composed.

(c) BCD multiplier

Basically, multiplier is achieved by repeating addition of a multiplicand by number of multiplier. The BCD multiplier is a circuit used to obtain same number of pulse outputs as number preset.

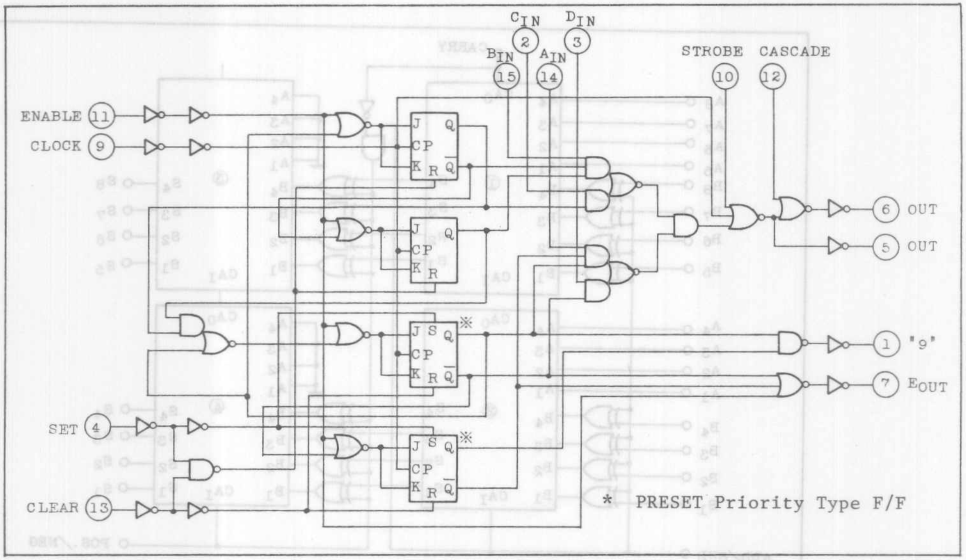


Fig. 2-205 TC4527BP BCD Rate Multiplier

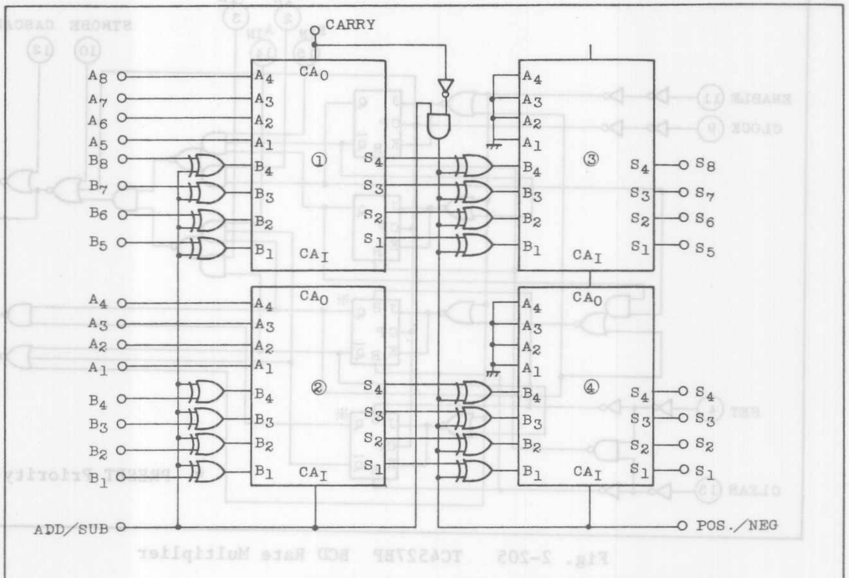
For instance, when addition of a multiplicand is repeated by number of outputs of a multiplier preset to the BCD multiplier, a result of multiplication is obtained as an output. TC4527BP outputs number of pulses corresponding to BCD input which is preset on a BCD multiplier.

As a matter of course, this TC4527BP can be also used as a programmable pulse generator/divider. In Fig. 2-205, the logic diagram of TC 4527BP is shown.

7.2 Application of arithmetic circuit

(1) Binary parallel adding/subtracting circuit

The 4 bit binary parallel adder TC4008BP is able to constitute a binary 4 x n bit adder when CARRY OUT is connected to CARRY INPUT of a host adder.



TC4008BP×4
TC4030BP×4
TC4011BP×1

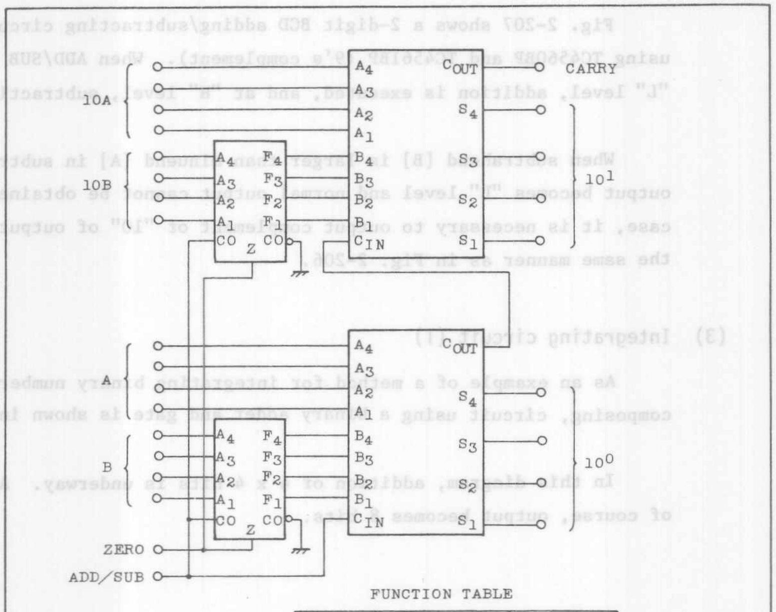
ADD/SUB	S_{OUT}	POS./NEG.
L	[A] + [B]	—
H	[A] − [B]	"L" Positive "H" Negative

Fig. 2-206 8-Bit Parallel Binary adding/subtracting circuit

Subtraction is achieved by adding 1's complement of a subtrahend and minuend. In this case, CARRY IN should be placed at "H" level. If CARRY IN is at "L" level, the result of subtraction is less by "1" as there is a demand for borrowing a digit from the lower digit.

Fig. 2-206 shows a binary 8 bit parallel adding/subtracting circuit. When ADD/SUB input is placed at "L" level, adding operation is executed and at "H" level, subtracting operation is executed.

When [A] data is larger than [B] data and [A] is equal to [B] in the subtracting operation, CARRY output becomes "H" level, and a result is obtained at ① and ② Adder outputs and therefore, ③ and ④ are not required.



ZERO	ADD/SUB	RESULT
L	L	A+B
L	H	A−B
H	*	A

Fig. 2-207 2-Digit BCD Adding/Subtracting Circuit

On the other hand, when [A] is less than [B],CARRY output becomes "L" level and digit borrowing from the upper digit is not possible and therefore, outputs ① and ② do not show the result of operation. In this case, ③ and ④ adders are required as 2's complement of output signal is output.

Needless to say, if a system is capable of making it an error if CARRY output indicates "L" level when [A] is less than [B], ③ and ④ are not necessary.

(2) BCD parallel adding/subtracting circuit

TC4560BP is a BCD adder. Subtraction is achieved by adding a minuend and complement of "9" of a subtrahend and by setting "H" level for CARRY input.

Fig. 2-207 shows a 2-digit BCD adding/subtracting circuit composed using TC4560BP and TC4561BP (9's complement). When ADD/SUB input is at "L" level, addition is executed, and at "H" level, subtraction is executed.

When subtrahend [B] is larger than minuend [A] in subtraction, CARRY output becomes "L" level and normal output cannot be obtained. In this case, it is necessary to output complement of "10" of output signal in the same manner as in Fig. 2-206.

(3) Integrating circuit (1)

As an example of a method for integrating binary numbers, a method composing, circuit using a binary adder and gate is shown in Fig. 2-208.

In this diagram, addition of 4 x 4 bits is underway. As a matter of course, output becomes 8 bits.

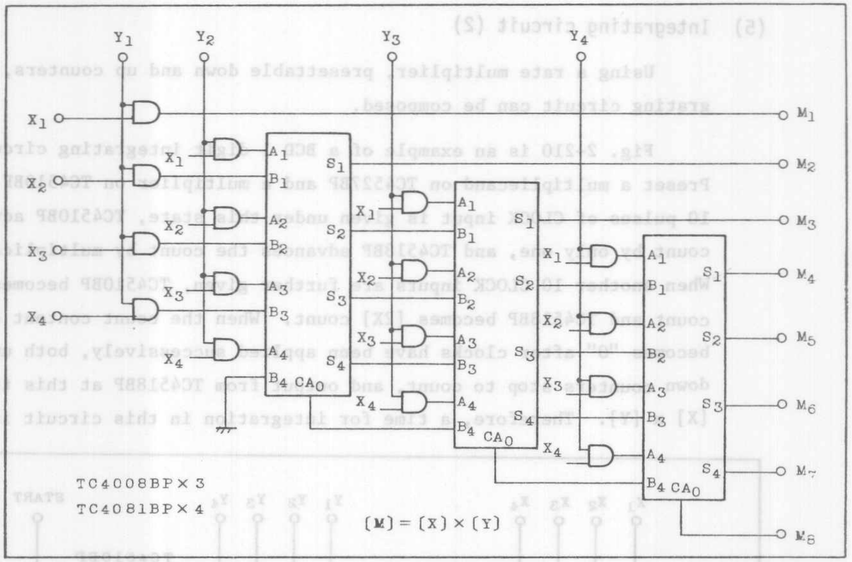


Fig. 2-208 Binary Adding Circuit Using Adder

(4) Cascade connection of BCD multiplier

When two BCD multipliers are cascade connected, output pulses ranging 0 ~ 99 can be obtained. Fig. 2-209 is an example of two TC4527BPs that are cascade-connected. In the same connection, n-digit BCD multiplier can be composed.

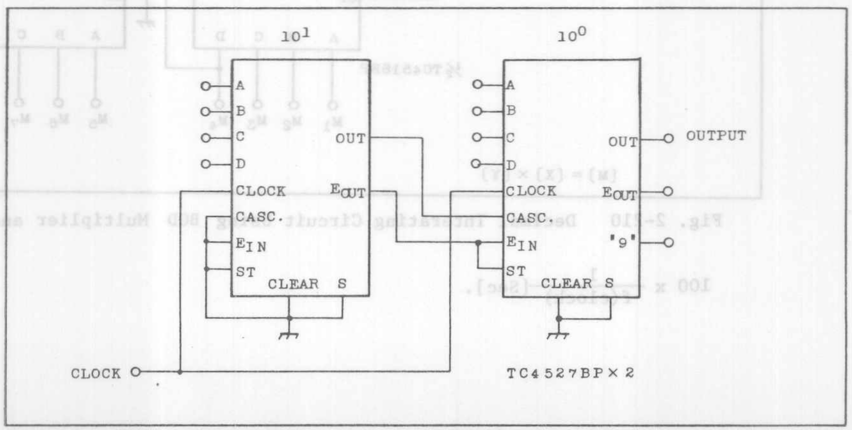


Fig. 2-209 Cascade Connection of BCD Multiplier

(5) Integrating circuit (2)

Using a rate multiplier, presettable down and up counters, an integrating circuit can be composed.

Fig. 2-210 is an example of a BCD 1 digit integrating circuit. Preset a multipliecand on TC4527BP and a multiplier on TC4510BP. When 10 pulses of CLOCK input is given under this state, TC4510BP advances the count by only one, and TC4518BP advances the count by multiplicand X. When another 10 CLOCK inputs are further given, TC4510BP becomes [Y-2] count and TC4518BP becomes [2X] count. When the count content of TC4510BP becomes "0" after clocks have been applied successively, both up and down counters stop to count, and output from TC4518BP at this time shows [X] x [Y]. Therefore, a time for integration in this circuit is max.

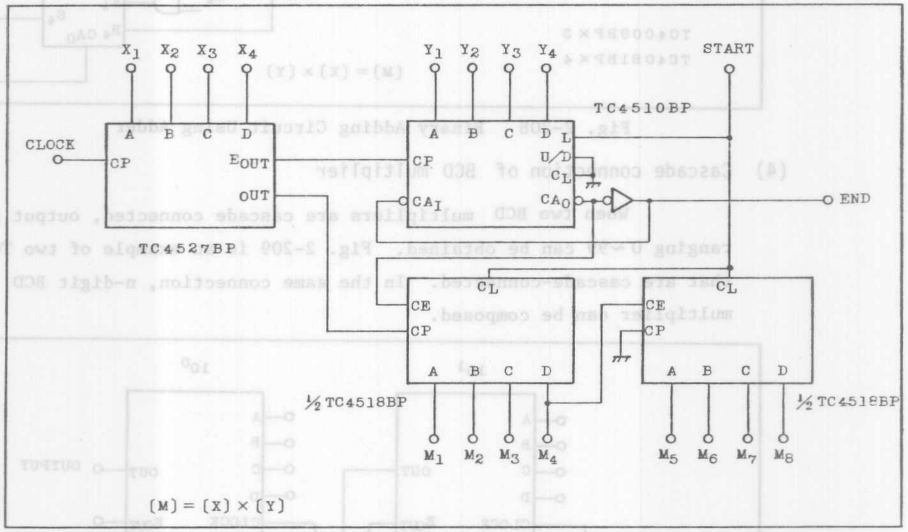


Fig. 2-210 Decimal Interating Circuit Using BCD Multiplier and Counters

$100 \times \frac{1}{f(\text{clock})}$ [Sec].

(6) Cascade connection of magnitude comparator

The magnitude/coincidence judging circuit for C^2MOS has TC4063BP and TC4585BP. These are 4-bit magnitude comparators, and n-units of comparator are cascade connected for expansion of number of bits as shown in Fig. 2-211 or Fig. 2-212.

As being capable of comparing either binary or BCD signal, these comparators have extremely broad range of applications.

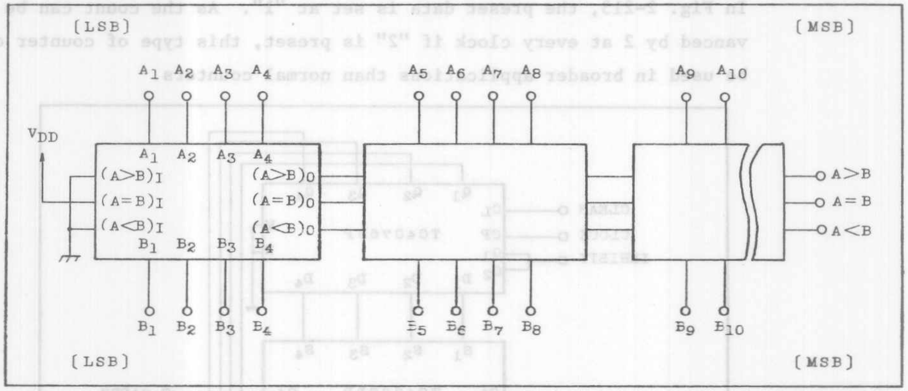


Fig. 2-211 Cascade Connection of TC4063BP

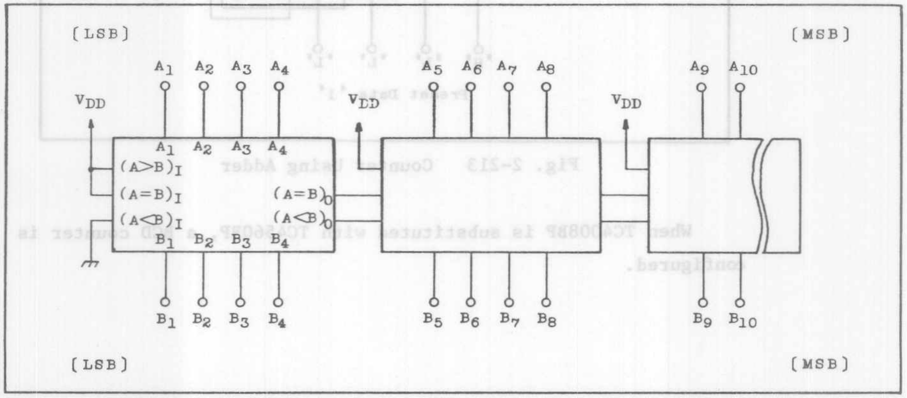


Fig. 2-212 Cascade Connection of TC4585BP

(7) Counter using adder and register

By connecting output of an adder to a register and returning the register output to the adder input, a counter can be composed. Shown in Fig. 2-213 is a binary up-counter with a binary adder and storage register used.

This counter counts up by one at every clock of TC4076BP.
In Fig. 2-213, the preset data is set at "1". As the count can be advanced by 2 at every clock if "2" is preset, this type of counter can be used in broader applications than normal counters.

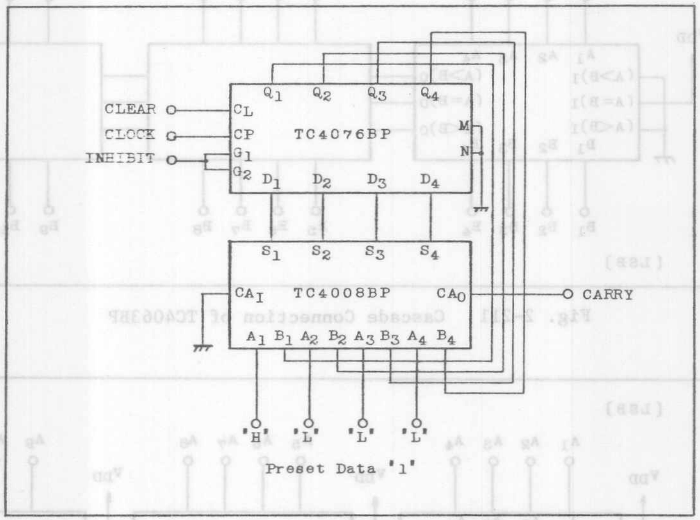


Fig. 2-213 Counter Using Adder

When TC4008BP is substituted with TC4560BP, a BCD counter is configured.

8. Other devices

There are several other unique products in C^2MOS family than those described in the foregoing. Some of these products are described in this section.

8.1 Multivibrator

TC4047BP is an astable multivibrator capable of deciding time constant through a capacitor and resistors that are externally attached. Output of this multivibrator becomes completely 50% duty cycle by the built in flip-flops.

Further, as oscillator output can be directly obtained, two frequency outputs f_{OSC} and f_Q can be obtained by constants C and R.

Frequency at the output terminal is expressed as shown below:

$$f_{OSC} \fallingdotseq \frac{1}{2.2CR}$$

$$f_{Q,\overline{Q}} \fallingdotseq \frac{1}{2 \times 2.2CR}$$

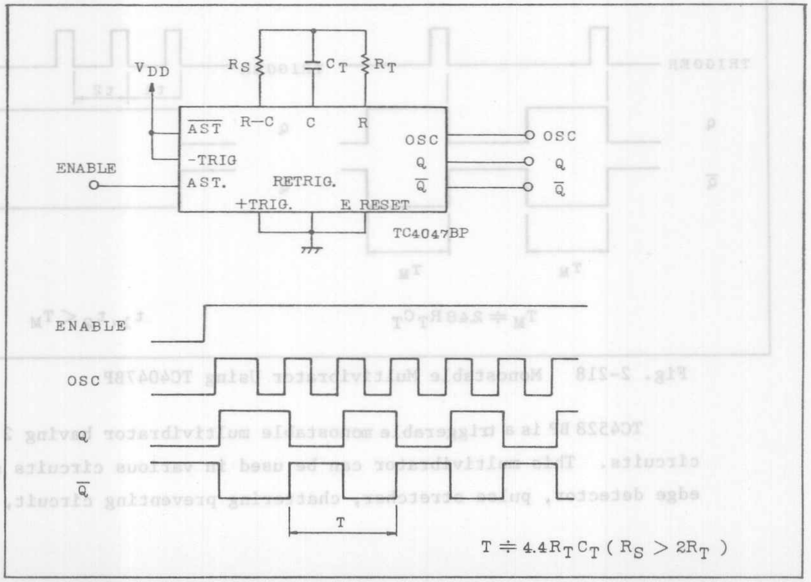


Fig. 2-217 Oscillation Circuit Using TC4047BP

TC4047BP can be used as a monostable multivibrator by changing its connection.

In Fig. 2-218, the basic connection of TC4047BP is shown. For trigger operation, + trigger retrigger input shall be connected.

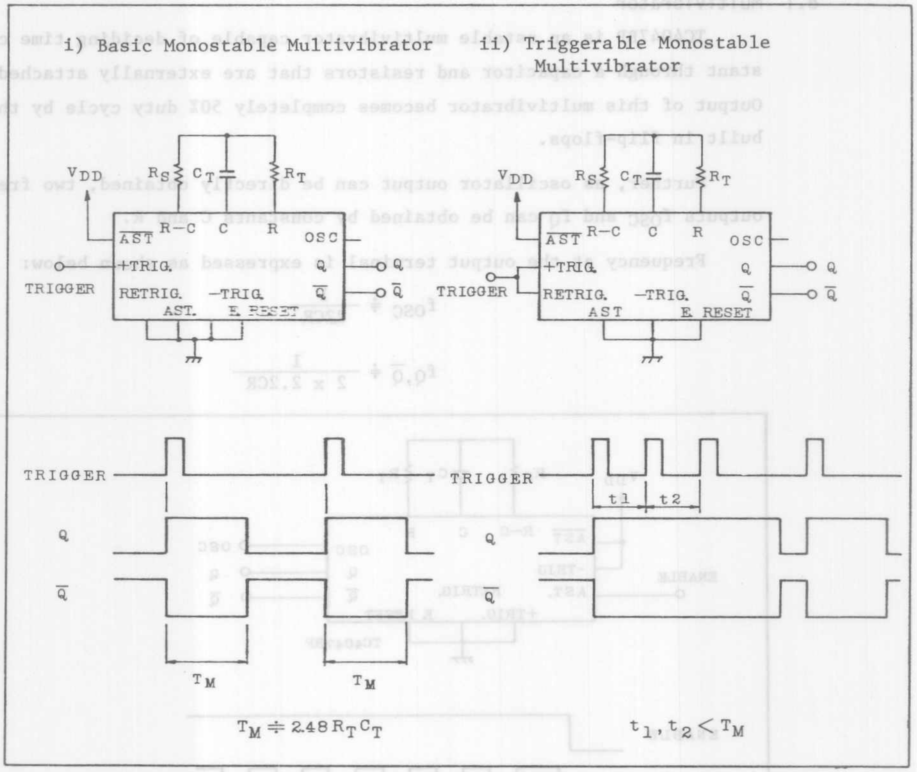


Fig. 2-218 Monostable Multivibrator Using TC4047BP

TC4528 BP is a triggerable monostable multivibrator having 2 built-in circuits. This multivibrator can be used in various circuits such as edge detector, pulse stretcher, chattering preventing circuit, etc.

8.2 TV Synchronizing signal generating LSI

TC5003P is a synchronizing signal generating LSI of 525/60 system color TV standard system (NTSC).

This LSI generates synchronizing signal, scanning signal, erase signal, etc. required for color TV camera and VIDEO camera.

In addition, various control signals required for TV camera are obtainable, this LSI is suited for making them in small size.

As power consumption is as less as 100 mV for color operation (14 MHz input) and 10 mV for white and black operation (2 MHz input), equipment can be powered by battery. This LSI is also most suited for generating synchronizing signal for CRT application circuits and TV games.

〔3〕 CHARACTERISTICS OF C^2MOS AND ITS INTERFACE

[3] CHARACTERISTICS OF C^2MOS AND ITS INTERFACE

1. Characteristics of C^2MOS

1.1 Current consumption

(1) Static current consumption

In C^2MOS IC, P-channel enhancement type (normally off type) FET and N-channel enhancement type FET are connected together so that they may constantly compensate each other. Namely, under the condition where the input voltage is stationary on V_{DD} or V_{SS} level, FET is certainly cut off in either P-channel type or N-channel type; therefore there is no passing of DC current flowing from V_{DD} to V_{SS}, with the exception of an extremely small leak current.

Thus, the supply current of input being fixed to V_{DD} or V_{SS} is called the static current consumption (Quiescent current consumption), and in C^2MOS IC, excepting special IC s, the worst value is guaranteed. Table 3-1 shows the standard guaranteed values in general SSI/MSI.

Table 3-1 Standard Guaranteed Values of C^2MOS IC Static Current Consumption

Classification	V_{DD}(V)	25°C MAX.	85°C MAX.	UNIT
GATE	5	1.0	7.5	µA
	10	2.0	15	
	15	4.0	30	
BUFFER F/F	5	4.0	30	µA
	10	8.0	60	
	15	16.0	120	
MSI	5	20.0	150	µA
	10	40.0	300	
	15	80.0	600	

In practice, the values of this static current consumption, which is structured only by PN junction saturation current in IC chip and chip surface leak current, are far small as compared with the standard values.

Fig. 3-1 shows the static current consumption characteristics of TC7400BP. From this figure it is clear that the static current consumption increases in the form of exponential function to the rise in ambient temperature. In the neighborhood of Ta=25°C, there are relatively large variation, but at the time of high temperature, such variations become small by focusing. This indicates that in normal temperature the surface leak or the like in addition to PN junction leak occupy a large portion, but that in high temperature the junction leak is dominant over all the others.

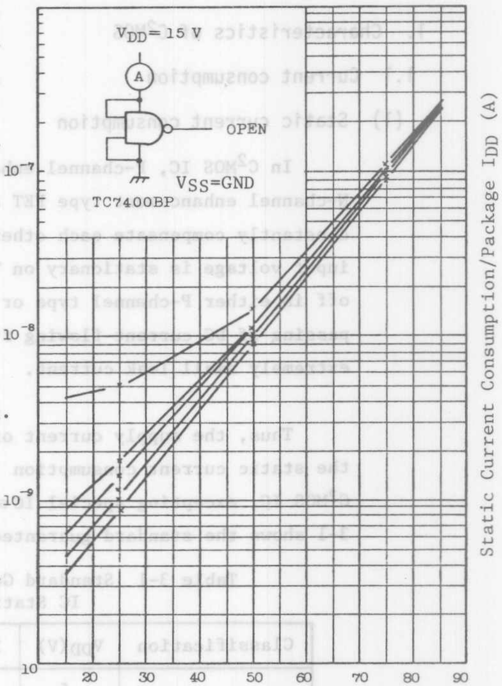


Fig. 3-1 Static Current Consumption of CMOS Gate

The static current consumption of MSI or others has a tendency similar to the above. However, the absolute value is considered to be proportional to the sum total of PN junction areas of IC chips rather than the number of IC internal elements. In MSI, the absolute value will be only about several times as large as that in gate IC.

(2) Operating current consumption

Usually, in case of using CMOS IC, as mentioned in (1) above, the input is connected neither to V_{SS} nor to V_{DD}, some pulse signals are given and also some pulse signals are sent as outputs.

In this case, if input signals are of an ideal step form, it follows that no DC current is in existance in the power supply, but that at the transition time of inversion of CMOS output current is in existance for charging and discharging the internal drain capacitance and load capacitance.

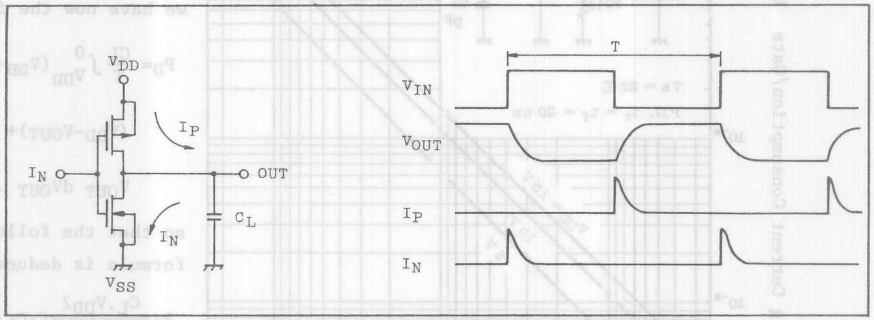


Fig. 3-2 Step Response of CMOS Inverter

Fig. 3-2 illustrates conceptionally such a state by quoting CMOS inverter as an example.

In the same figure, the sum total of IC internal capacitance, wiring capacitance, etc. is considered as C_L in the approximation. In the case of the inversion of CMOS output from "L" to "H", the actual output voltage cannot rise unless the load capacitance is charged to V_{DD}. Therefore, it follows that the charge equivalent to $C_L V_{DD}$ is supplied by V_{DD} through P-channel FET.

The above sets forth the reason for the flow of I_P in case of output rising from "L" to "H" in Fig. 3-2.

Quite similary, in case of falling of output from "H" to "L", there exists the pulse current flowing in V_{SS}. The loss by these currents (power consumption) is obtained by integrating the transient power for one cycle when the cycle of input pulse is expressed by T.

Then $P_D = \frac{1}{T}\int_0^T I_P\cdot(V_{DD}-V_{OUT})dt + \frac{1}{T}\int_0^T I_N\cdot V_{OUT}\, dt$ .... (3-1)

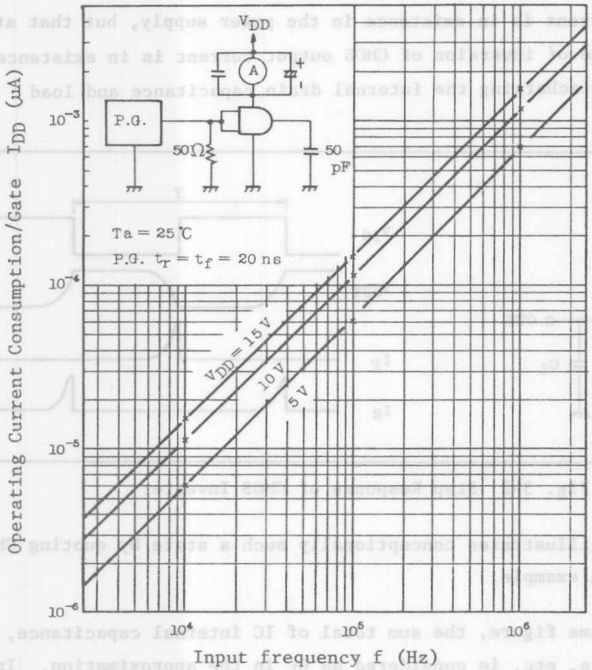


Fig. 3-3 Operating Current Consumption of TC4081BP

hence,

$$I_P = C_L \cdot \frac{d(V_{DD}-V_{OUT})}{dt},$$

$$I_N = C_L \cdot \frac{dV_{OUT}}{dt}$$

we have now the formula

$$P_D = \frac{CL}{T} \int_{V_{DD}}^{0} (V_{DD}-V_{OUT})\,d(V_{DD}-V_{OUT}) + \frac{CL}{T} \int_{V_{DD}}^{0} V_{OUT}\,dV_{OUT} \quad \ldots (3\text{-}2)$$

so that the following formula is deduced:

$$P_D = \frac{C_L \cdot V_{DD}^2}{T} = f \cdot C_L \cdot V_{DD}^2 \quad ..(3\text{-}3)$$

As is clear from the formula (3-3), the current consumption of CMOS is proportional to the square of input frequency, load capacitance and supply voltage.

Fig. 3-3 shows the characteristics of input frequency and operating current consumption in the case of making the load capacitance constant by using 2-input NAND gate, TC4081BP.

As is clear from the same figure, the current consumption is only about 1 mA even when the input frequency is 1 MHz, and this bespeaks the fact that low power consumption capacity is fully displayed in the application field where the input frequency is below 1 MHz.

Every in logic circuits such as MSI, etc., the power consumption is proportional to the input frequency in quite the same as mentioned before.

In general, however, the load capacitance in the internal circuit of IC is extremely small as compared with that in the output terminal, whereby in many cases the internal loss may be ignored as compared with the loss in output buffer.

Therefore, in reality the current consumption seems to be decided accroding to the number of output terminals in operation (under inversion), which is taken as a criterion.

With MSI, the output frequency rarely corresponds to the input frequency at the ratio of 1 to 1, and the output frequency is divided severally. This is one of the factors for lowering the loss of MSI.

In the actual MSI, the power consumption is about several times as much as that of gate IC.

(3) Current consumption by input waveforms other than square waveforms

From the propagation characteristic formula of inverter described in 2.2 (1) of Chapter I, the operating area of CMOS inverter is broadly classified into three domains as illustrated in Fig. 3-4:

I) $0V \leqq V_{IN} \leqq V_{TN}$ .... (3-4)

II) $V_{TN} \leqq V_{IN} \leqq V_{DD} - |V_{TP}|$ .... (3-5)

III) $V_{DD} - |V_{TP}| \leqq V_{IN} \leqq V_{DD}$ .... (3-6)

In the domains of I) and III), either of N-channel FET and P-channel FET is cut off. In the domain of II), however, both FETs are turn On.

[The domain of II) is further divided into three domains depending on the fact that each FET operates in the saturation area or in the non-saturation area. On this point, explanation is omitted here.]

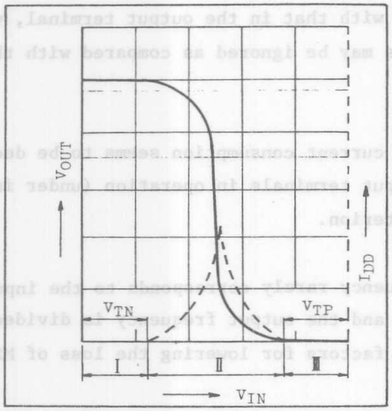


Fig. 3-4 Voltage Characteristics of CMOS Inverter

Namely, when the input voltage of the CMOS inverter is situated on the intermediate level between V_{SS} and V_{DD}, DC current flows from V_{DD} terminals to V_{SS} terminals. For example, in the crystal oscillation circuit feedback from the output to the input of CMOS inverter through resistors, and in the simple type amplifier, the input is always on the intermediate level requiring larger power for a CMOS. The same may be said of the circuits processing gentle waveforms such as integrating/differentiating circuit, oscillation circuit, etc. using capacitors and resistors.

Fig. 3-5 shows the supply current characteristics of HEX INVERTER TC4069BP, while Fig.3-6 shows the supply current characteristics of gate TC4011BP with buffer. As is clear from Fig. 3-6, since the gate with buffer has a shaping action in the preceding stage circuit, the DC current is less than that of the one stage gate.

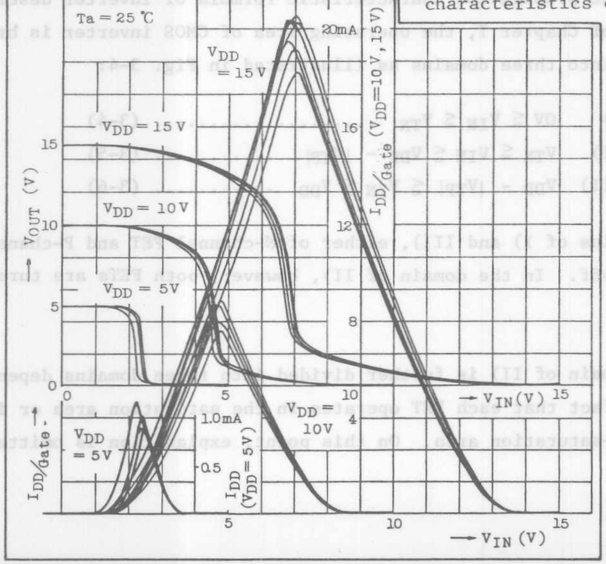


Fig. 3-5 V_{IN} - V_{DD} Characteristics of TC4069UBP

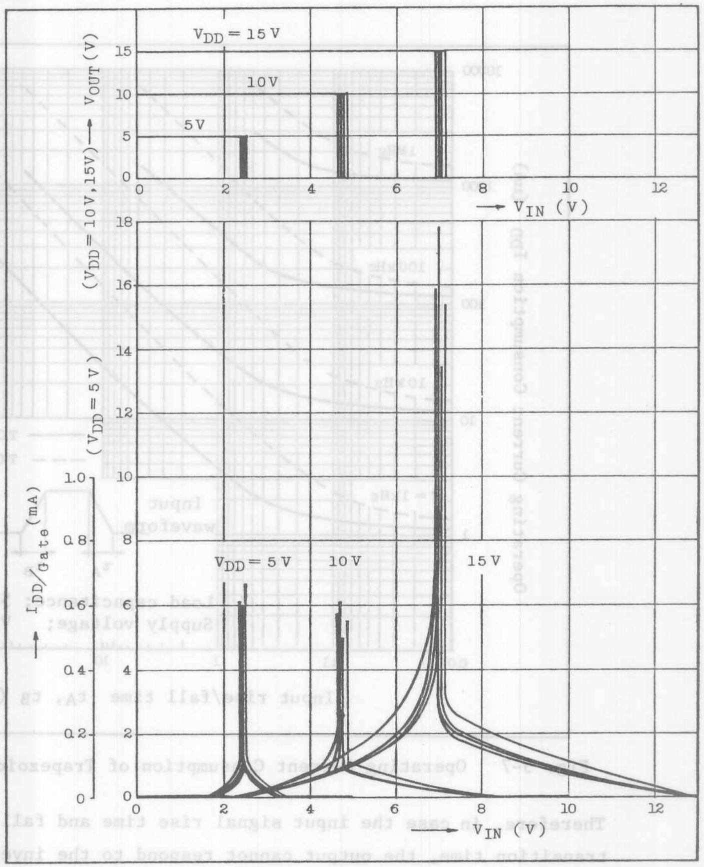


Fig. 3-6 V_{IN} - I_{DD} Characteristics of TC4011BP

Generally, in MSI and the like, the transfer characteristic is close in shape to that shown in Fig. 3-6. Namely, in C^2MOS, DC peak current flows at the transition time in inversion of inverter at the output stage. However, in Fig. 3-5 and Fig. 3-6, I_{DD} is measured by changing the input voltage relatively slowly.

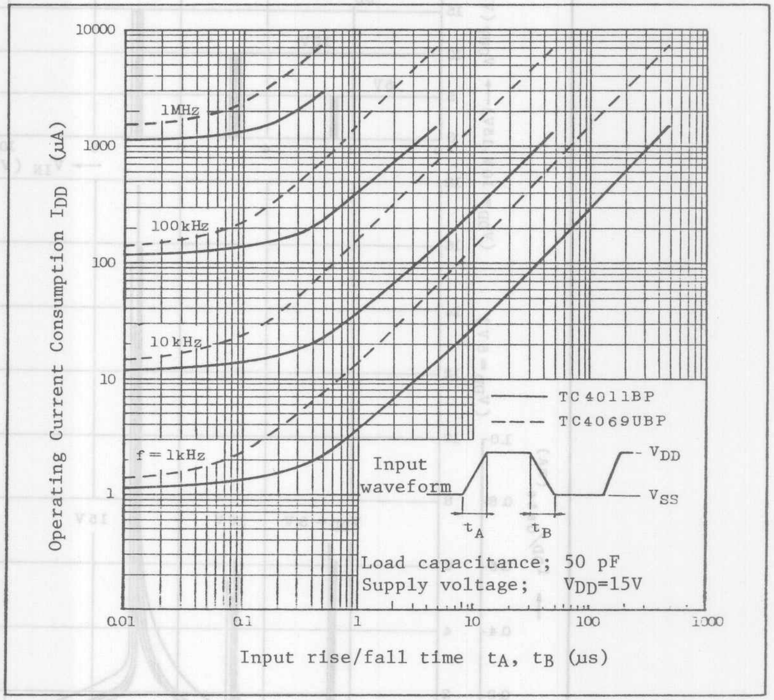


Fig. 3-7 Operating Current Consumption of Trapezoidal Input Waveform

Therefore, in case the input signal rise time and fall time are very short transition time, the output cannot respond to the inversion action of FET, V_{IN}-I_{DD} characteristics is applied the current characteristics at the time when the square wave input has been given.

Fig. 3-7 shows average supply current characteristics in the case of having given the trapezoidal waves to the inputs of TC4069UBP and TC4011BP. As is clear from the Fig., at the one-stage gate of TC4069BP, etc., it is necessary to consider DC current effect to the input waveforms which have rise time and fall time exceeding 100 ns. Further, in the three state gate represented by TC4011BP, the boundary is the range of approx. 300 ns - 500 ns.

1.2 Input characteristics

(1) Input protection circuits

In C^2MOS IC, the protection circuits with resistors and diodes are inserted in all the inputs for protecting the gate oxidation film from static electricity. Fig. 3-8 shows C^2MOS input protection circuits.

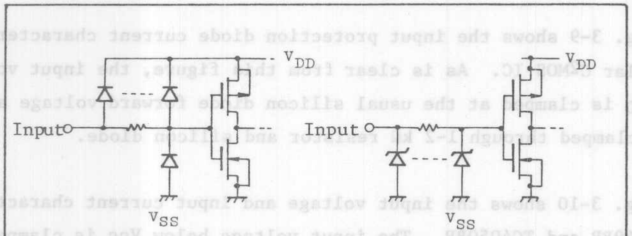


Fig.3-8 C^2MOS Input Protection Circuits

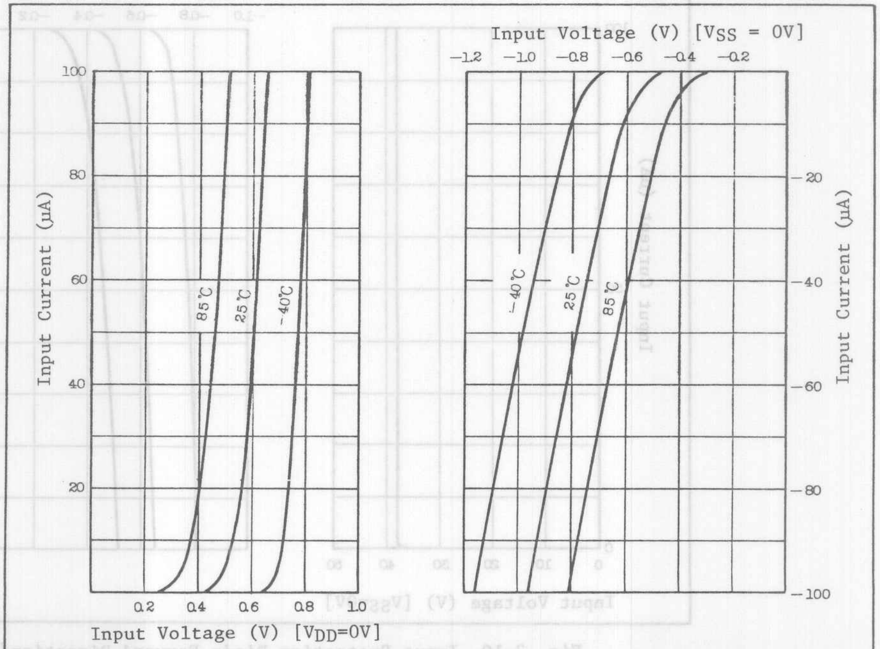


Fig. 3-9 Input Protection Diode Forward Characteristics (Protection Circuit I)

For the two kinds of products, TC4049BP and TC5040BP, which are provided with the level shifter function, the circuit (b) in the same figure is adopted, while the circuit (a) in the same figure is inserted in all the C^2MOS IC inputs.

Fig. 3-9 shows the input protection diode current characteristics of regular C^2MOS IC. As is clear from this figure, the input voltage over V_{DD} is clamped at the usual silicon diode forward voltage and under V_{SS} is clamped through 1-2 kΩ resistor and silicon diode.

Fig. 3-10 shows the input voltage and input current characteristics of TC4049BP and TC4050BP. The input voltage below V_{SS} is clamped by silicon diode, but for higher input voltage this protection diode breaks down at V_{SS} + (30～40)V.

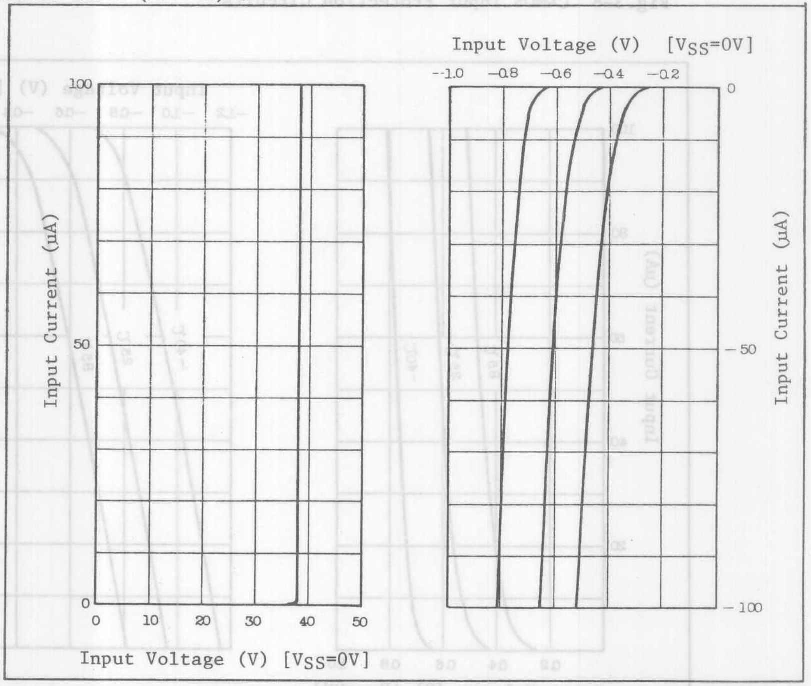


Fig. 3-10 Input Protection Diode Forward Direction/ Inverse Direction Characteristics (Protection Circuit II)

These input protection diodes are not used to flow current like the usual switching diode. In designing the system, therefore, it is essential to use these input protection diodes within the rating of $V_{SS} - 0.5V \sim V_{SS} + 20V$ in case the input voltage is usually $V_{SS} - 0.5V \sim V_{DD} + 0.5V$ for TC4049BP and TC4050BP. Even when current flows in these diodes, consideration shall be given to keeping the current value at $1 \sim 2$ mA or below.

(2) Input impedance

For the input voltages ranging from V_{SS} to V_{DD}, all the protection diodes are in the state of inverse bias, therefore, the input impedance of CMOS is extremely high, and is only $10^{-4} \sim 10^{-5}$ (μA) calculated in terms of leak current.

Thus, for actuating CMOS IC, unlike other bipolar devices, no current matching is required. Extremely speaking, CMOS IC can operate on any voltage level.

However, the input terminal of CMOS is of capacitive ($3 \sim 5$PF) type by reason of configuration, and in the actual interface fanout is frequently restricted at the said capacitive value.

(3) Threshold voltage (V_{THC}) and noise immunity

In CMOS IC, this circuit threshold voltage (V_{THC}) is defined by the input voltage value when the output voltage comes to 1/2 V_{DD}.

Ideally, the design is made so that the V_{THC} may come to 1/2 V_{DD}. In reality, however, the decision is made by P-channel and N-channel ON resistance ratio, whereby there are some variations in the initial characteristic, influenced directly by the variations of these FETs. Fig. 13-11 shows the data for variations of QUAD2-INPUT NAND gate TC4011BP.

As shown in the same figure, in NAND/NOR gate the V_{THC} changes more or less depending on the connection method. For example, the input terminals, etc. of inverter and MSI have a similar degree of variation width. This variation shows the difficulty in application of CMOS IC to analog comparator/level slicer without externally additional circuit.

However, V_{THC} is relatively stable to temperatures and the shift width can be ignored as compared with the variation in initial characteristics.

Fig. 3-12 shows V_{THC} temperature characteristics of TC4011BP. As is clear from this figure, the temperature coefficients of V_{THC} are approx. -2 ~ 3 mV/°C (at V_{DD}=5V) and -4 ~ -6 mV/°C (at V_{DD}=10V).

As mentioned above, there are variations in the initial characteristics of V_{THC} of CMOS IC; therefore, the guaranteed levels are specified to high level input voltage (V_{IH}) and low level input voltage (V_{IL}) of products.

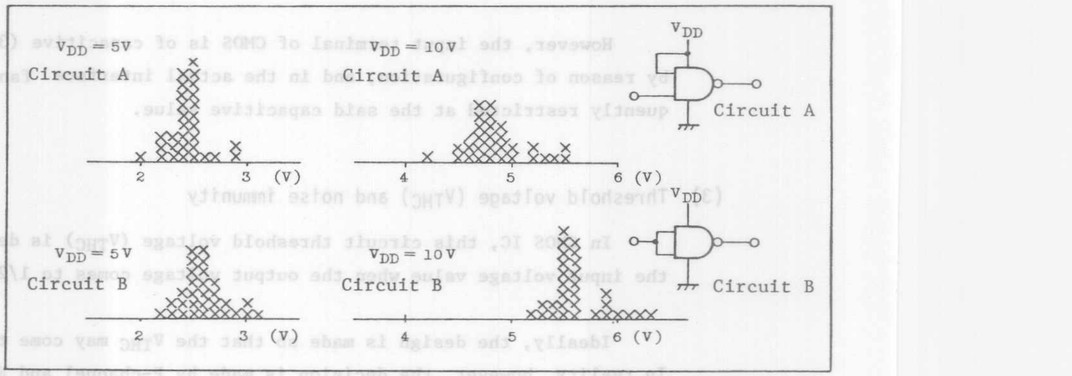


Fig. 3-11 Examples of V_{THC} Variations of TC4011BP

V_{IH} (min) and V_{IH} (max) are guaranteed for all the products of C^2MOS IC, so that it is essential to use the products within the range of V_{IH} (min) to V_{DD} on "H" level and within the range of V_{SS} to V_{IL} (max).

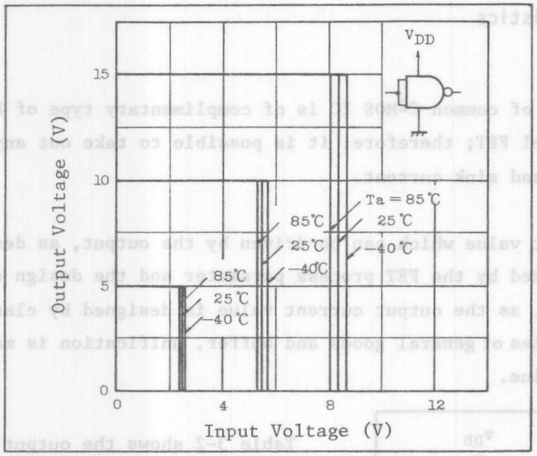


Fig 3-12 Input/Output Voltage Characteristics of TC4011BP

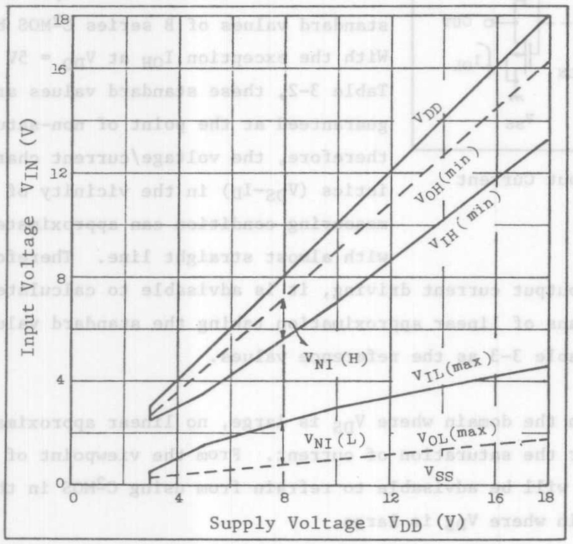


Fig.3-13 Noise Immunity of "B" Type C^2MOS IC

Namely, it is guaranteed that V_{THC} is within the range of V_{IL} (max) to V_{IH} (min), and C^2MOS IC products are essentially different from the products, such as comparator and the like.

Fig. 3-13 shows the noise immunity of C^2MOS IC. The noise immunity V_{NI} is expressed by the following formulas;

$$V_{NI}(H) = V_{OH}(min) - V_{IH}(min) \quad \ldots (3\text{-}7)$$

$$V_{NI}(L) = V_{IL}(max) - V_{OL}(max) \quad \ldots (3\text{-}8)$$

In the case of "B" type C^2MOS, the same value is guaranteed to $V_{NI}(H)$ and $V_{NI}(L)$.

If $V_{NI}=V_{NI}(H)=V_{NI}(L)$,

$$\begin{cases} V_{NI} = 1V(min)/@V_{DD} = 5V \\ V_{NI} = 2V(min)/@V_{DD} = 10V \\ V_{NI} = 2.5V(min)/@V_{DD} = 15V \end{cases}$$

1.3 Output characteristics

(1) Output current

The output of common C^2MOS IC is of complimentary type of P-channel FET and N-channel FET; therefore, it is possible to take out any of source current and sink current.

The current value which can be driven by the output, as described in [1], is decided by the FET process parameter and the design constant. In C^2MOS family, as the output current value is designed by classifying it into two series of general goods and buffer, unification is made on the standard value.

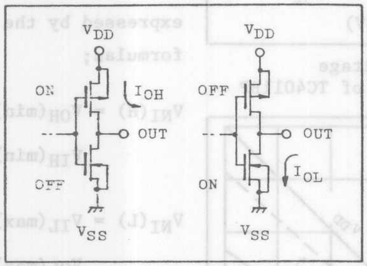


Fig. 3-4 Output Current

Table 3-2 shows the output current standard values of B series C^2MOS IC, while Table 3-3 shows the output current standard values of B series C^2MOS buffer. With the exception I_{OH} at V_{DD} = 5V in Table 3-2, these standard values are all guaranteed at the point of non-saturation; therefore, the voltage/current characteristics (V_{DS}-I_D) in the vicinity of measuring condition can approximate with almost straight line. Therefore, at the time of output current driving, it is advisable to calculate the worst V_{DS} by means of linear approximation taking the standard values in Table 3-2 and Table 3-3 as the reference values.

However, in the domain where V_{DS} is large, no linear approximation is permitted for the saturation of current. From the viewpoint of power consumption, it will be advisable to refrain from using C^2MOS in the saturation domain where V_{DS} is large.

Table 3-2 Output Current Specifications of B Series C^2MOS (General Products)

ITEM	SYMBOL	TEST CONDITIONS	SPECIFIED MIN. VALUE			UNIT
			−40°C	25°C	85°C	
High Level Output Current	I_{OH}	$V_{DD}=5V$, $V_{OH}=4.6V$	−0.2	−0.16	−0.12	mA
		$V_{DD}=10V$, $V_{OH}=9.5V$	−0.5	−0.4	−0.3	
		$V_{DD}=15V$, $V_{OH}=13.5V$	−1.4	−1.2	−1.0	
Low Level Output Current	I_{OL}	$V_{DD}=5V$, $V_{OL}=0.4V$	0.52	0.44	0.36	mA
		$V_{DD}=10V$, $V_{OL}=0.5V$	1.3	1.1	0.9	
		$V_{DD}=15V$, $V_{OL}=1.5V$	3.6	3.0	0.2	

Table 3-3 Output Current Specifications of B Series C^2MOS (Buffer)

ITEM	SYMBOL	TEST CONDITIONS	SPECIFIED MIN. VALUE			UNIT
			−40°C	25°C	85°C	
High Level Output Current	I_{OH}	$V_{DD}=5V$, $V_{OH}=2.5V$	−1.4	−1.25	−1.0	mA
		$V_{DD}=10V$, $V_{OH}=9.5V$	−1.4	−1.25	−1.0	
		$V_{DD}=15V$, $V_{OH}=13.5V$	−4.0	−3.75	−3.0	
Low Level Output Current	I_{OL}	$V_{DD}=5V$, $V_{OL}=0.4V$	3.5	3.2	2.5	mA
		$V_{DD}=10V$, $V_{OL}=0.5V$	6.0	5.0	3.6	
		$V_{DD}=15V$, $V_{OL}=1.5V$	26.0	24.0	18.0	

Fig. 3-15 and Fig. 3-16 show the output current characteristics (standard values) of the representative buffer TC4049BP and gate TC4011BP.

As is clear from the same figure, output current decreases by approx. 15%~20% in the state of high temperature as compared with the normal temperature condition.

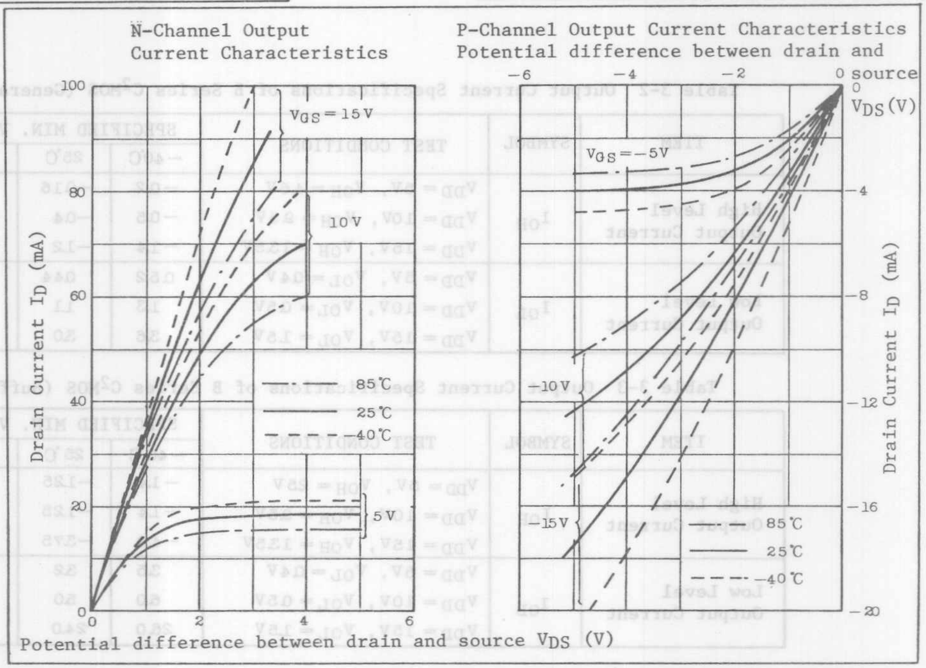


Fig. 3-15 Output Current Characteristics of TC4049BP

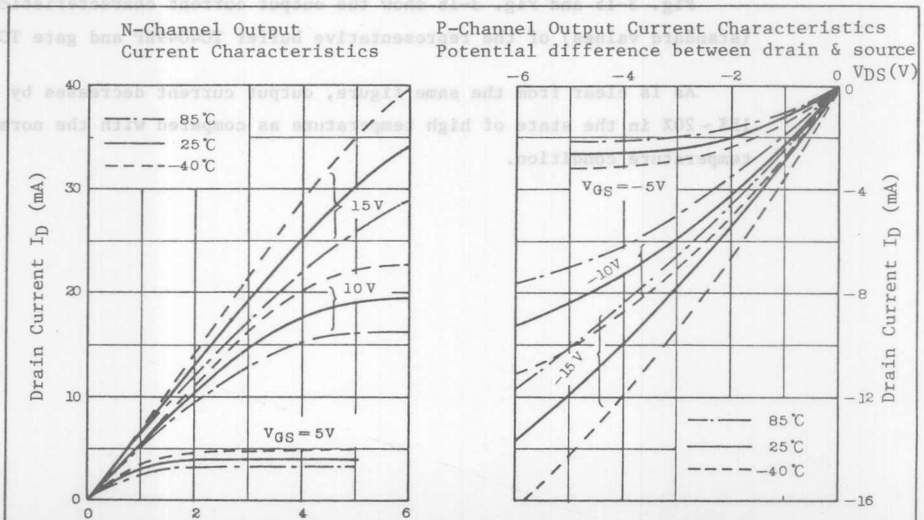


Fig. 3-16 Output Current Characteristics of TC4011BP

(2) Three-state output

Usually, C^2MOS IC produces the outputs in the complimentary type shown in (1). In case the outputs are connected together directly, the current flows from "H" level output to "L" level output as shown in Fig. 3-17. Such output connection should be absolutely avoided, partly because the meaningless power is consumed and partly because the loss may exceed the permissible loss when the supply voltage is high.

The above is not desirable because the excessive circuits are required at the time of connection of bus line and C^2MOS IC as the I/O port or at the time of trying to reduce the number of parts.

Three-state output is the circuit provided with the three kinds of states, two kinds of states of "H" and "L" plus the high impedance state where both P- and N-channels come to OFF. When these state outputs are connected together each another, if one of the outputs is arranged for high impedance, current doesn't flow between outputs.
This makes it possible directly to connect the outputs.

Fig. 3-18 shows an example of three-state output circuit. The outputs of TC4508BP(4-BIT LATCH) and TC5012BP(HEX 3-STATE BUFFER) can perform three-state operation. The number of terminals which can be

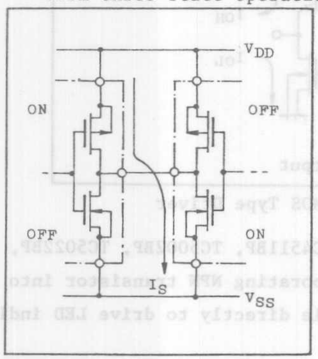


Fig.3-17 Connection of Outputs

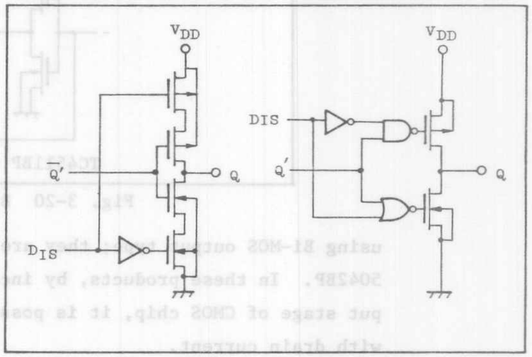


Fig.3-18 Example of Three-state Output Circuit

connected together directly with three-stage outputs is decided by three-state leak current, I_{OH} and I_{OL}.

In reality, however, it will be advisable to use approx. 10 terminals in consideration of the delay in switching time because the disable output (high impedance output) has a capacitance of approx. 15 PF per piece.

(3) Open drain output, Bi-MOS output

C^2MOS IC has TC5029BP, TC5030BP, TC5064BP, TC5065BP, TC5066BP, and TC5067BP which are provided with the open drain output capable of conducting level and wired OR in addition to (1) and (2). These products shows the general output current characteristics in the case of output FET being ON, but since no current flows until they reach the drain breakdown voltage in the case of output FET being OFF, this makes it possible to carry out the conversion of logical level.

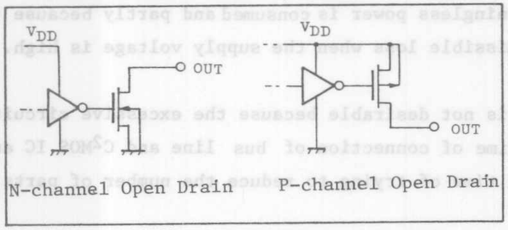


Fig. 3-19 Open Drain Output System

For the current driving device like LED lighting, bipolar type output is more effective than MOS transister. In C^2MOS, there are LED drivers using Bi-MOS output type; they are TC4511BP, TC5002BP, TC5022BP, and TC 5042BP. In these products, by incorporating NPN transistor into the output stage of CMOS chip, it is possible directly to drive LED indicator with drain current.

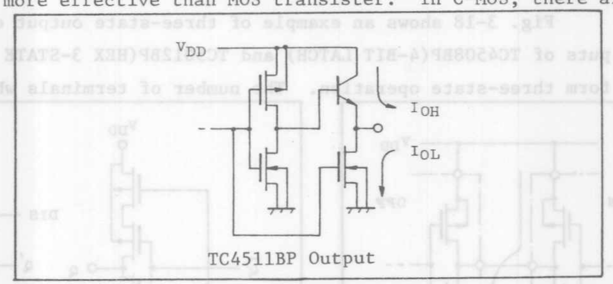


Fig. 3-20 Bi-MOS Type Driver

However, by reason of circuit construction this NPN bipolar transistor is of emitter follower type; therefore, the voltage corresponding to Base-Emitter Voltage of NPN transistor drop. Namely, for drawing out the output current I_{OH}, the output voltage, V_{DD}-V_{BE} or below, is required.

1.4 Switching characterisitcs

(1) Propagation delay time

The propagation delay time of MOS IC is decided by the drain current characteristics (ON resistance) of internal FET and the capacitances formed in each part of the device. In general, the larger the number of gate stages connected between input and output, the larger the delay time becomes.

The propagation delay time of C^2MOS IC is defined by high level propagation time (t_{PLH}) and low level propagation time (t_{PHL}). The former is the transition time requiring for inversion from "L" level to "H" level with the response of output after input, and the latter is the transition time requiring for the output inverted from "H" level to "L" level.

These propagation times vary depending on the supply voltage (V_{DD}-V_{SS}), load condition (load capacitance), input waveform condition, etc. In measuring, therefore, it is required to define these parameters.

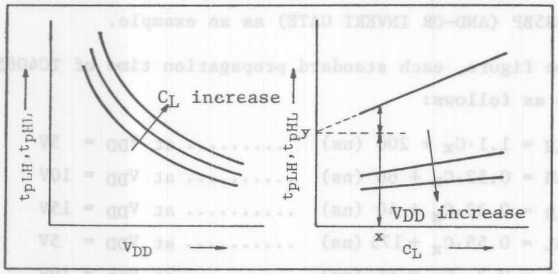


Fig. 3-21 Propagation Time of C^2MOS IC

Fig.3-21 shows the example of characteristics of V_{DD}-t_{PLH}, t_{PHL} in case the load capacitance is constant and the example of characteristics of C_L-t_{PLH}, t_{PHL} in case V_{DD} is constant.

As seen from the figure, the propagation time increases linearly to the increase of load capacitance. This shows that the propagation time is expressed by the following formula:

$$t_{PLH},\ t_{PHL} = Ax + y \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (3\text{-}9)$$

x ; C_L (pF)

y ; Propagation time (ns) C_L=0

A ; Capacitance dependency of propagation time (ns/pF)

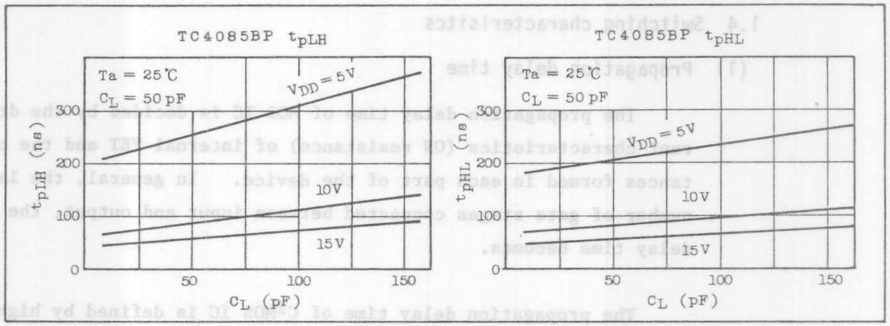


Fig. 3-22 Propagation Time of C^2MOS IC (TC4085BP)

Namely, the first term of (3-9) formula represents the delay in output response characteristic by load capacitance and the second term represents the internal delay.

Fig. 3-22 shows the standard propagation time characteristics by quoting TC4085BP (AND-OR INVERT GATE) as an example.

From the same figure, each standard propagation time of TC4085BP at Ta = 25°C is as follows:

$t_{pLH} = 1.1 \cdot C_x + 200$ (ns) .... at V_{DD} = 5V
$t_{pLH} = 0.52 \cdot C_x + 60$ (ns) .... at V_{DD} = 10V
$t_{pLH} = 0.33 \cdot C_x + 40$ (ns) .... at V_{DD} = 15V
$t_{pHL} = 0.55 \cdot C_x + 175$ (ns) .... at V_{DD} = 5V
$t_{pHL} = 0.3 \cdot C_x + 65$ (ns) .... at V_{DD} = 10V
$t_{pHL} = 0.2 \cdot C_x + 45$ (ns) .... at V_{DD} = 15V

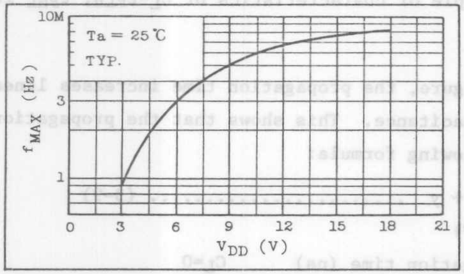


Fig.3-23 $f_{MAXØ}$ Characteristics of TC4027BP

Returning to formula (3-9), it is found that the coefficient A in the formula is inversely proportional to the current driving capacity of output buffer.

The temperature characteristics of each propagation time have relations with the temperature characteristics of output current,

and comes to approx. 120% of normal temperature at high temperature (85°C) and also comes to approx. 80% of normal temperature at low temperature (-40°C).

(2) Max. clock frequency ($f_{MAX\emptyset}$)

In the products which have clock input such as flip-flop, counter, shift regist, etc., there is the max. value of clock input frequency.

In C^2MOS family, these products are of static operation with the exception of some products, therefore, the clock input frequency conditions range from DC to $f_{MAX\emptyset}$.

Actually, the max. clock frequency is defined in the separate data sheet; therefore, the products have to be used at the standard value or below.

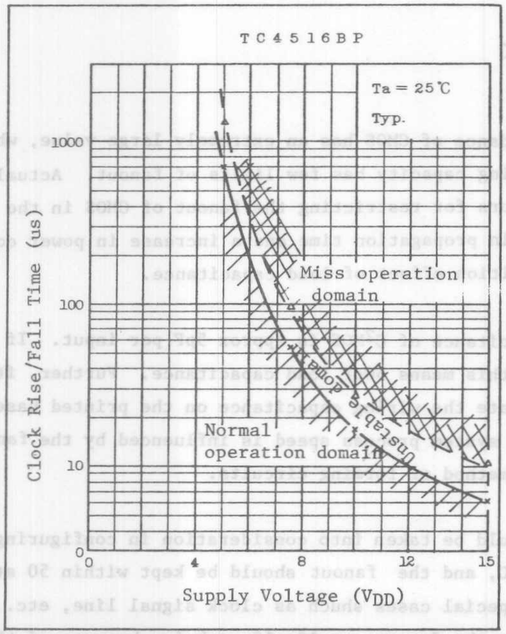


Fig. 3-24 Clock Rise and Fall Times

Fig. 3-23 shows the max. clock frequency characteristics of TC4027BP (DUAL J-K FLIP FLOP).

(3) Max. Clock rise time and fall time

As the flip-flop of CMOS holds the data by changing over the internal switch, if the switch change-over operation is not performed as expected, the operation of master stage does not correspond to the operate of slave stage, whereby erroneous operation is caused.

In the flip-flop C^2MOS, the change over of internal gate is carried out by the clock input signals (CP and $\overline{CP}$). If the rise time and fall time of clock signals become long, the divergency of phase is caused in CP signal and $\overline{CP}$ signal, resulting in miscount and racing.

As the clock input rise and fall times by products are prescribed in the data sheet, it is necessary to input clock signals which have rise and fall transition time characteristics within the standard value.

Fig. 3-24 shows the clock rise and fall time threshold characteristics, quoting TC4516BP as an example. It is necessary to pay particular attention to the shaping of clock at the domain where supply voltage is high.

2. Interface

2.1 Interface of C^2MOS IC

(1) Fanout of C^2MOS

The input impedance of CMOS has an extremely large value, whereby at the current driving capacity has few limits of fanout. Actually, therefore, the factors for restricting the fanout of CMOS in the system will be a decrease in propagation time and a increase in power consumption due to the addition effect of load capacitance.

The input capacitance of C^2MOS is approx 5pF per input. If the fanout is ten pieces, this means 50pF load capacitance. Further, it is necessary to calculate the wiring capacitance on the printed base board. This shows that the system process speed is influenced by the fanout in addition to the method of forming circuits.

This point should be taken into consideration in configuring a system with C^2MOS IC, and the fanout should be kept within 50 at the maximum. In the special cases shuch as clock signal line, etc. it will be advisable to keep the fanout at 10 ~ 15 or below because of the limits of rise time and fall time.

(2) Input output interface

In case some processing is made with CMOS systems almost all of the systems communicate with external circuits and mechanisms through signals. In many cases, these input and output signal lines are long and they themselves have the distributing inductance and reactance. Therefore, if they are directly connected to CMOS, it may cause many troubles.

Concretely speaking, the greatest troubles will be malfunction by induced noise and breaking of input and output elements by surge. For the former, the measures are taken so as to lower the signal line impedance (driving impedance) and to insert the noise removal circuit in the receiving side. For the latter, surge protection countermeasures are taken.

Fig. 3-25 shows the noise surge protection made on the input side. In the fig., (a) and (b) are the examples for absorbing noises by integrating input waveform by R and C. In same figure, (c) and (d) are the examples of protecting C^2MOS from the input surge.

Fig.. 3-26 shows an example of output interface. These are only few examples. In any case, in general the interface with long signal lines is protected in some way or other.

(3) Interface with separate power supply system

In case of connecting C^2MOS systems operating by separate power supply, if input and output of CMOS are connected directly, disorder may occur, even though the two supply voltages are same.

This is because the difference in rise time and fall time in the two power supplies may cause the possiblility of generating the state where the CMOS input voltage receiving signals transiently exceeds the rating.

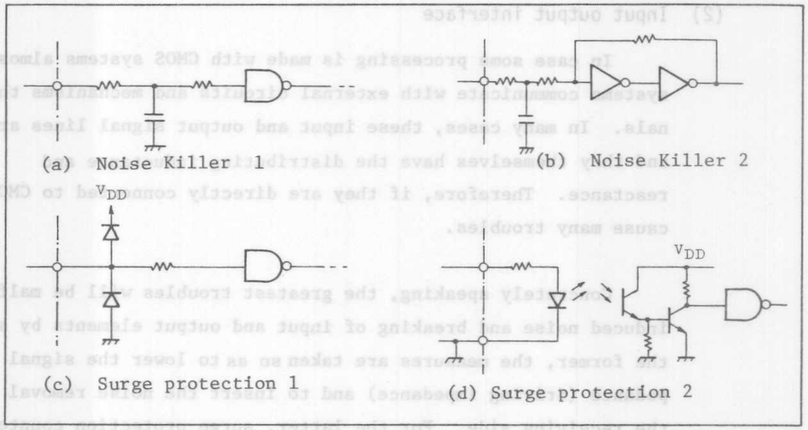


Fig. 3-25 Examples of C²MOS Input Protection Circuit

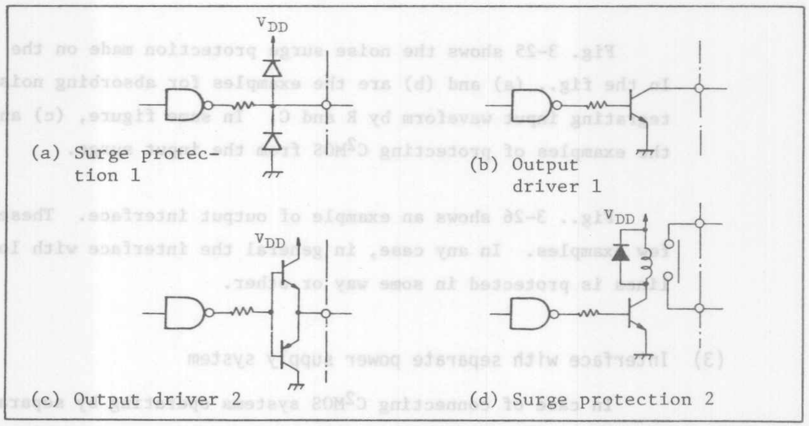


Fig. 3-26 Output Protection/Drive Circuit

Fig. 3-27 shows the example. The waveform "1" in the figure has no problem because the relation of $V_{DD2} > V_{DD1}$ is always established. In waveforms "2" and "3", the state of $V_{DD1} > V_{DD2}$ is generated. In such a state, if the signal line is on "H" level, the current i flows through the input protection diode of CMOS with mark*.

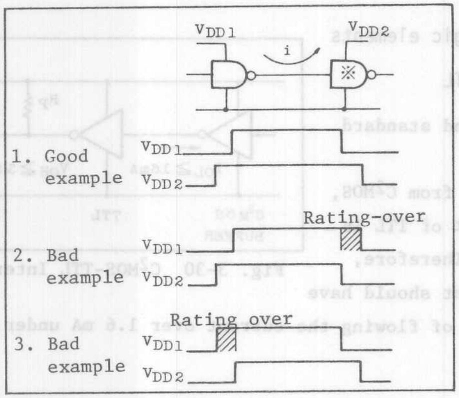


Fig.3-27 Two-Power Supply Interface

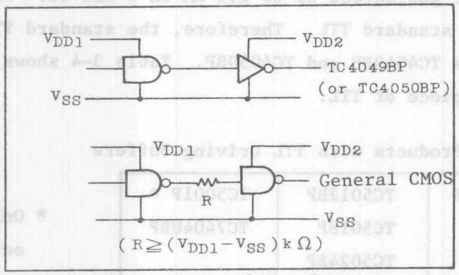


Fig.3-28 Example of Two-Power Supply Interface

TC4049BP and TC4050BP are capable of performing the level conversion from high voltage system to low voltage system, while TC5020BP is capable of conducting the level conversion from low voltage system to high voltage system.

Fig. 3-29 shows the example of interface using these devices. The level conversion can be made by pulling up or pulling down the open drain output, such as TC5029BP, TC5030BP, etc. through resistors.

This current can cause the deterioration in circuit with mark* and the latch-up. It is advisable, therefore, to use TC4049BP or TC4050BP which has special input protection circuit as shown in Fig.3-28.

In case it is impossible to use the above circuit in Fig.3-28, current limt resistance shall be inserted in series in the signal line as shown under Fig.

(4) Logical level converter

In many cases the separate power supply system interface usually requires the logic level converting function. In C^2MOS, therefore, TC4049BP, TC4050BP and TC5020BP are available as the logic level converters.

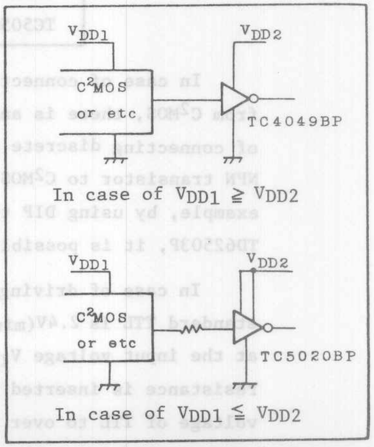


Fig.3-29 Logical Level Converter

2.2 Interface with other logic elements

(1) Interface with TTL/LSTTL

(a) Connection of C^2MOS and standard TTL

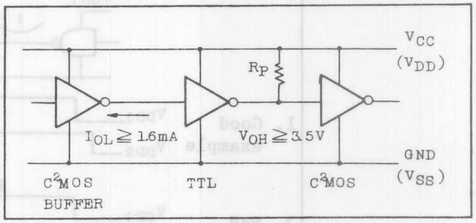


Fig. 3-30 C^2MOS-TTL Interface

In case of driving TTL from C^2MOS, the "L" level input current of TTL is defined at max. -1.6 mA. Therefore, the low level output current should have the specifications capable of flowing the current over 1.6 mA under the condition of V_{OL} = 0.4V.

In general, I_{OL} is not guaranteed up to 1.6 mA in C^2MOS IC. This makes it impossible to drive the standard TTL. Therefore, the standard TTL is driven through the buffers such as TC4049BP and TC4050BP. Table 3-4 shows the buffers capable of connecting one piece of TTL.

Table 3-4 Products with TTL Driving Buffers

TC4009UBP	TC5012BP	TC5001P *
TC4010BP	TC5018P	TC7404UBP
TC4049BP	TC5024BP	
TC4050BP	TC5025BP	
TC5000P	TC5029BP	
TC5050P	TC5050BP	

* Only BCD output

In case of connection of TTL from C^2MOS, there is another method of connecting discrete or monolisic NPN transistor to C^2MOS output. For example, by using DIP transistor allay TD62503P, it is possible to drive TTL from C^2MOS as shown in Fig. 3-31.

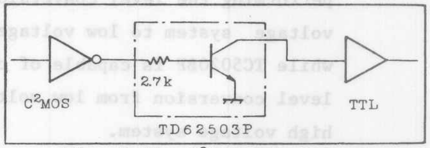


Fig. 3-31 C^2MOS-TTL Interface

In case of driving C^2MOS from TTL, as the high level output voltage of standard TTL is 2.4V(min.), the transfer of "H" level comes to impracticable at the input voltage V_{IH} (min.)=3.5V of C^2MOS. Therefore, usually the pull-up resistance is inserted between V_{CC} and output for raising the high level voltage of TTL to over 3.5V.

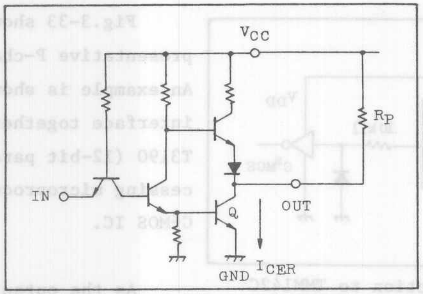


Fig.3-32 Pull-up of TTL Output

The pull-up resistance value is decided by the leak current I_{CER} at the time of OFF of output transistor Q of TTL. This value is not guaranteed for the usual TTL. However, from the guarantee level of open collector TTL, it is estimated that the max. 250μA will be sufficient. In order to make the voltage drop by Rp (5-3.5)=1.5V or below, it follows that;

$$Rp = \frac{1.5}{0.25} \times 10^3 = 6 \ (k\Omega)$$

Accordingly, approx. 3 ~ 5 kΩ seem to be usually selected.

In the case of open collector TTL, the driving is carried out through the pull-up resistors in the same conception as mentioned above.

(b) Interface of C^2MOS and LSTTL

In the case of LSTTL, fundamentally, the connection is made in the same conception as the standard TTL. IN LSTTL,however, I_{IL} is as small as 0.4 mA (max.), so that one piece of LSTTL can be driven directly from usual C^2MOS. In buffer C^2MOS, it is possible to directly drive up to 4 pieces of LSTTL. In case of driving C^2MOS from LSTTL, the connection is made through 3 ~ 5 kΩ pull-up resistors in the same manner as the standard TTL.

(2) Interface with MOS LSI

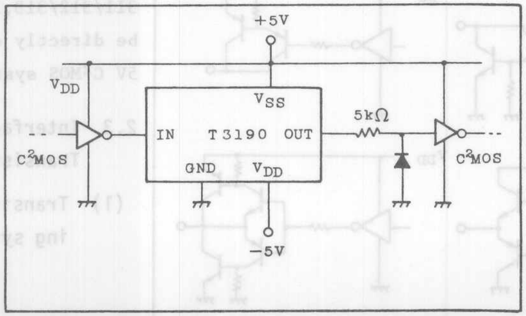


Fig. 3-33 Connection to T3190

P-channel/N-channel MOS LSIs are different in supply voltage and input/output specifications depending on products; therefore, it is necessary to compose the interface circuit suitable for the device.

Fig.3-33 shows the representative P-channel LSI. An example is shown on the interface together with T3190 (12-bit parallel processing microprocessor) and C^2MOS IC.

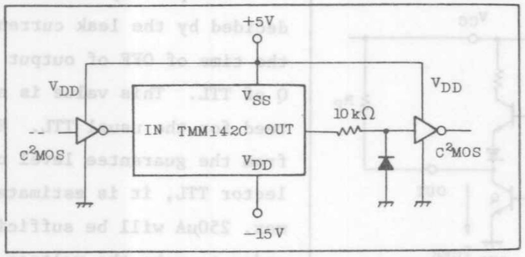


Fig. 3-34 Connection to TMM142C

As the output of T3190 deflects up to the minus side, in case C^2MOS is driven, it is necessary to clamp the output at 0V. Fig.3-34 shows the interface side of MNOS memory TMM142C.

In the case of TMM142C, the output also swings up to the minus side, and this makes it necessary to construct the clamping circuit.

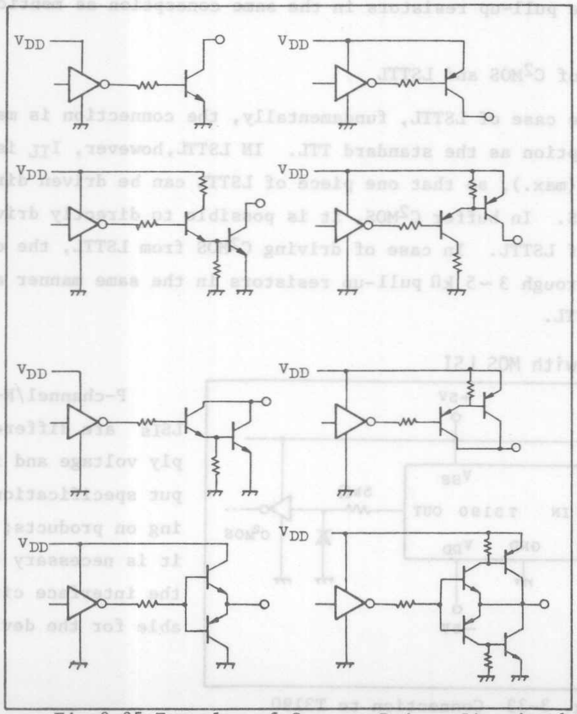


Fig.3-35 Examples of Current Driver Circuits by Transistors

Most N-channel MOS LSIs are 5V single power supply systems, and both input and output can be connected to C^2MOS as they are. Toshiba's N-cheannel static RAM memories, TMM 311/312/313,314P, etc.can be directly connected to 5V C^2MOS systems.

2.3 Interface with Transistor

(1) Transistor driving system

The output of C^2MOS can take out both sink current and sorce current; therefore, the interface with transistor is easily made.

Fig.3-35 shows an example of the current driving circuit using PNP/NPN transistors. These circuits are effective for driving relay, lamp LED, etc. which cannot be driven by output current of C^2MOS.

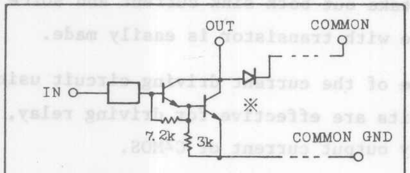
And the open collector type driving method is used for the conversion of the above-mentioned logic level and the driving of fluorescent indication tube.

(2) Transistor allay

Table 3-5 Table of Toshiba's Transistor Allays

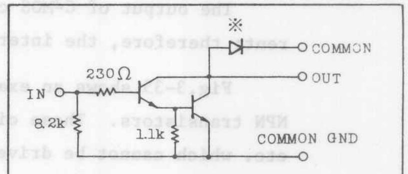
Name	I_C	$V_{CE(SUS)}$ (V_{CEO})	h_{FE}	CIRCUIT	Base Circuit	Clamping Diode	Dwg.
TD62001P	500mA	35V	1000 min	Darlington 7-circuit	—	Built-in	A
TD62002P					10.5kΩ+7V(ZENOR)		
TD62003P					2.7kΩ		
TD62004P					10.5kΩ		
TD62064P	1500	35	800 (typ)	Darlington 4-circuit	As shown in the of next page Fig.	[a]	B
TD62074P						[b]	
TD62101P	500	25	1000 min	Darlington 7-circuit	—	[b]	A
TD62103P					2.7kΩ		
TD62104P					10.5kΩ		
TD62105P					20.0kΩ		
TD62107P	750	45	—	Darlington 4-citcuit	TTL condition	[a]	C
TD62301P	200	15	1000	Darlington 7-circuit	2kΩ	[a]	D
TD62302P					8.4kΩ		
TD62501P	200	35	70	Single 7-circuit	—	[b]	E
TD62502P			50		10.5kΩ+7V(ZENOR)		
TD62503P					2.7kΩ		
TD62504P					10.5kΩ		
TD62505P			70				F
TD62506P					2.7kΩ		
TD62507P				Single 5-circuit	—		G

Note) [a] = Built-in [b] = Not built-in



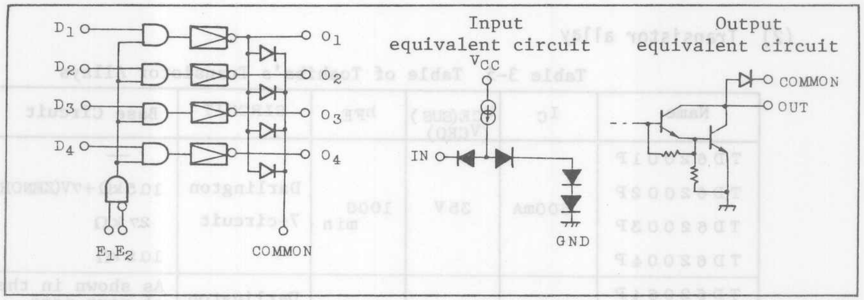
* Only TD62001P Series

A) TD62001P~TD62004P
TD62101P~TD62105P

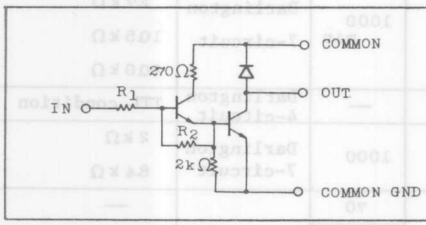


* Only TD62064P

B)TD62064P , TD62074P

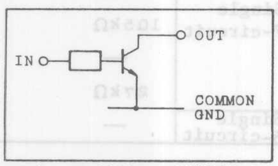


C) TD62107P

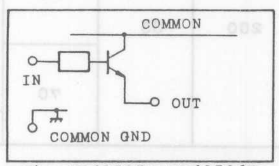


	R_1	R_2
TD62301P	2k	20k
TD62302P	8.4k	15k

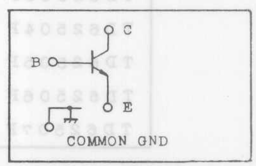
D) TD62301P, TD62302P



E) TD6250 ~ T62504P



F) TD62505P,TD62506P



G) TD62507P

Available for using these drivers are DIP 16-pin type driver allays as shown in Table 3-5. That is, available are various types ranging from single NPN transistor allays (TD62501 series) to high voltage resisting large current driving Darlington allays (TD62064/62074) and these products are optimum to the output drivers of C^2MOS.

Table 3-5 shows the list of these driver ICs.

2.4 Interface with mechanical contact

(1) Chattering of mechanical contact

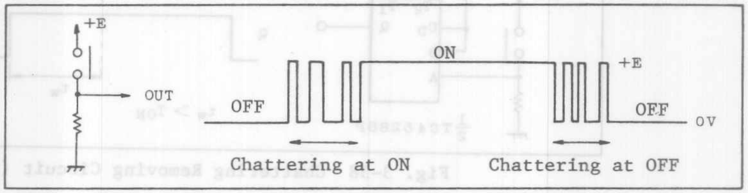


Fig. 3-36 Chattering Phenomenon

In General, in the mechanical contacts of relay, switch, etc. there is a contact bouncing phenomenon called chattering. In case "ON" and "OFF" of contact are converted into electric signals, the bouncing becomes a signal as it is as shown in Fig. 3-36. Namely, in case the contact once becomes "ON" ("OFF"), several times of "ON" and "OFF" signals are caused. Usually, as to the contact interface, chattering removal circuit is inserted in the electronic circuit.

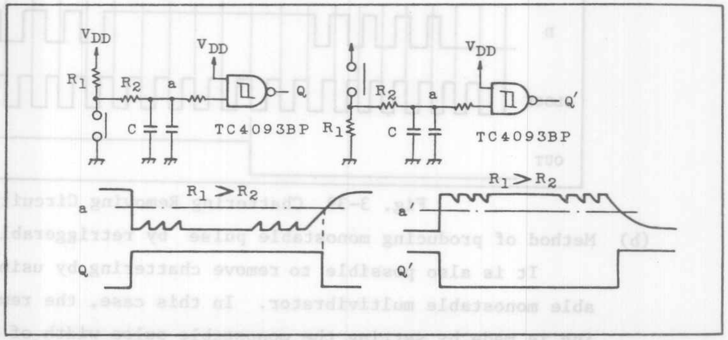


Fig. 3-37 Chattering Removing Circuit (1)

(2) Chattering removing circuit (2-terminal contact)

(a) Method of integrating signal waveform by capacitor and resistor

Fig. 3-37 is an example of the circuit for removing chattering by integrating signal waveform by capacitor and resistor. As the integrating time of signal is decided by the time constant

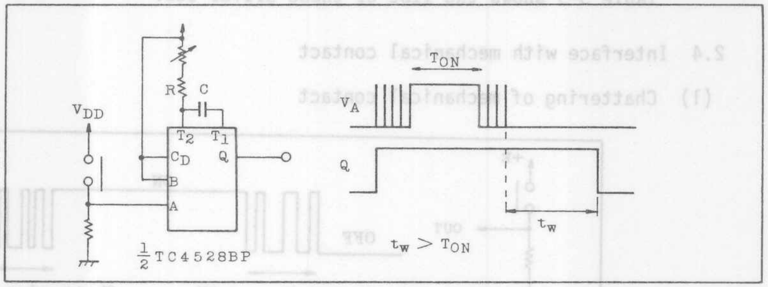


Fig. 3-38 Chattering Removing Circuit (2)

and C, it is necessary to select the constant matching the chattering time of switch.

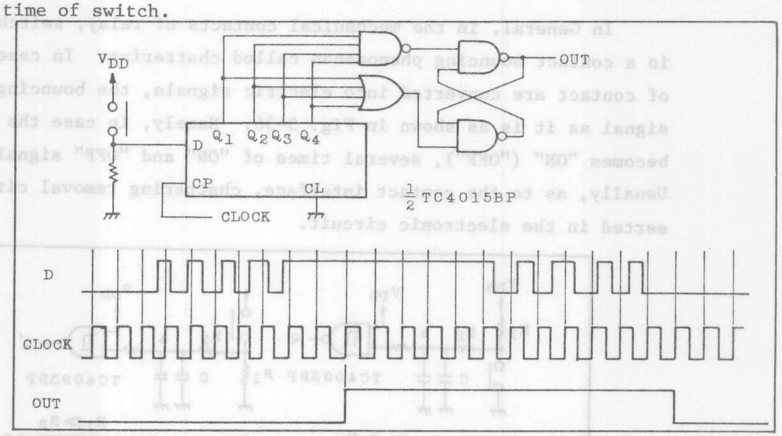


Fig. 3-39 Chattering Removing Circuit (3)

(b) Method of producing monostable pulse by retriggerable monomulti

It is also possible to remove chattering by using the retriggerable monostable multivibrator. In this case, the removal of chattering is made by setting the monostable pulse width of monomulti larger than the switch "ON" time (T_{ON}).

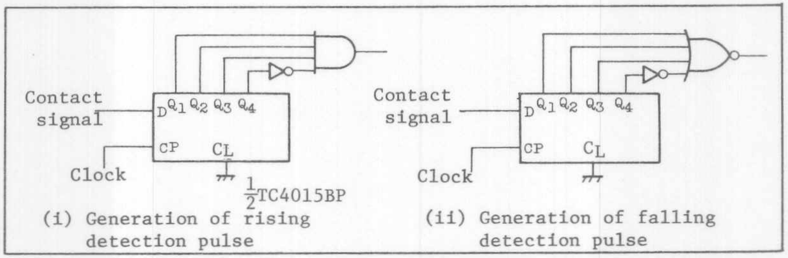


Fig. 3-40 Shaping Circuit

(c) Shaping by the shift register

In the methods (a) and (b), chattering is removed by using the passive elements. Fig. 3-39, however, shows the circuit sending the output of "ON" at the several continuance of "H" level and sending the output of "OFF" at the several continuance of "L" level by sampling the input data by use of the shift register.

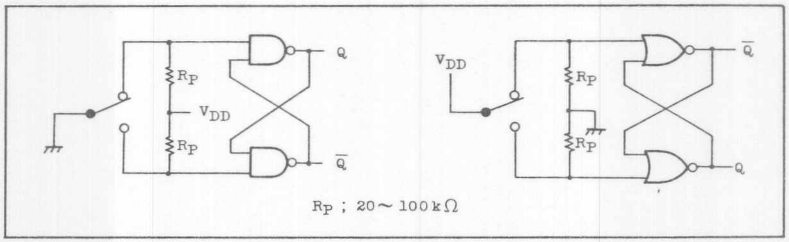


Fig. 3-41 Chattering Removing Circuit by R-S Flip-Flop

For converting the contact signal into the electric signal more simply, available is a method of sending the output of one clock by the shift register and gate IC as shown in Fig. 3-40.

(3) Chattering removing circuit (3-terminal contact)

In the case of 3-terminal contact, chattering can be removed relatively simply.

Fig.3-41 shows the circuit preventing output from inversion by using R-S flip-flop when the contact is in the intermediate state being not any side.

Fig. 3-40 Shaping Circuit

(c) Shaping by the shift register

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〔4〕 CAUTIONS ON HANDLING

[4] CAUTIONS ON HANDLING

By reason of its configuration, C^2MOS IC behaves itself in the manner different from Bipolar Logic centering around the conventional TTL. Although C^2MOS IC has many advantages over TTL, unsuitable method of use may result in the failure of full use of these advantages. In this chapter explanation is made on the cautions in handling C^2MOS IC and the cautions in designing circuits by using C^2MOS IC.

1. Configuration of C^2MOS necessary to know before handling and designing

C^2MOS IC input is connected to the gate electrode of MOS configuration having extremely thin oxide. As shown in Fig. 1, MOS configuration is defined in general as the sandwich configuration consisting of metal, oxide and semiconductor.

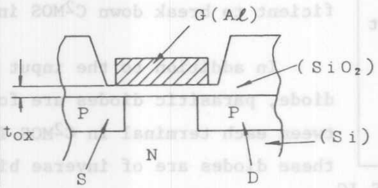


Fig. 1 MOS Configuration
(Example of P-Channel MOS)

The thickness (tox) of oxide insulator located directly under the gate electrode is usually as thin as $0.1 \sim 0.2\mu$; therefore, even when the voltage of $100V \sim 200V$ is applied between gate and N-substrate the electric field strength of oxide insulator just under the gate reaches as large as $10^7 V/cm$, causing dielectric breakdown by discharge.

For protecting the gate from the above-mentioned dielectric breakdown, TOSHIBA C^2MOS IC is provided at each input terminal with the protective circuit consisting of diode and resistor as shown in Fig. 2. According to the same figure, the voltage applied to the input terminal is clamped by D_1 and D_2 at V_{DD} and V_{SS}, whereby the input gate is protected. However, the input protective circuit has its limit.

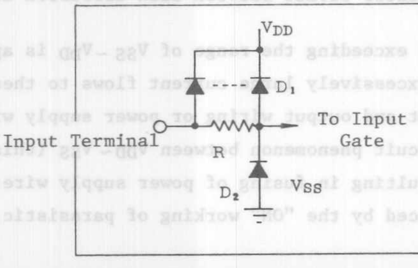


Fig. 2 Input Protection Circuit

As an example, the static electricity remaining in the fibers by the friction of fibers and needle of industrical sewing machine for synthetic fibers or that generated by men and women walking on a carpet may reach several kV ~ some dozen kV, though the voltage differs depending on relative humidity and surface condition.

The above-mentioned static electricity is stored in the storing case of fibers or in human body, which is equivalent to the fact that the above-mentioned voltage is charged to the electrostatic capacity or human body capacity (200 ~ 300PF). When this electric charge discharges to C^2MOS input, it is transformed into the energy sufficient to break down C^2MOS input.

In addition to the input protective diode, parasitic diodes are formed between each terminal in C^2MOS IC, and all these diodes are of inverse bias at the voltage within the max. rating.

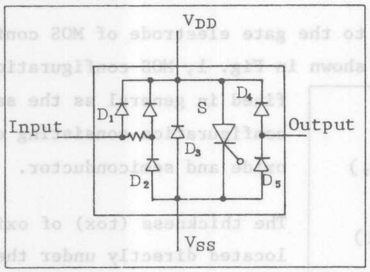


Fig. 3 Parasitic circuit of C^2MOS IC

However, when the voltage exceeding the max. rating is applied between each terminal, excessively large current flows to these diodes.

Fig. 3 shows the parasistic circuit formed between each terminal of C^2MOS IC. In same figure, D_1 and D_2 are the input protective diodes, D_3 is the diode formed by P-well diffusion, D_4 is the diode by the drain formation of P-channel MOS FET, and D_5 is the diode by the drain formation of N-channel MOS FET. S is the parasistic thyristor formed between each diffusion area.

For example, when the voltage exceeding the range of $V_{SS} \sim V_{DD}$ is applied to C^2MOS input or output and the excessively large current flows to these diodes, firstly the fusing of input and output wiring or power supply wire will occur and secondly, short-circuit phenomenon between $V_{DD} \sim V_{SS}$ (this is generally called the Latch-up, resulting in fusing of power supply wire as the destruction mode) will be induced by the "ON" working of parasistic thyristor.

Therefore, it is necessary to use the voltage on input and output terminals within the rating without fail.

2. Cautions on Handling C^2MOS IC

2.1 Transportation and storing

The input and output of C^2MOS IC which is not actually installed are in the state of high impedance. It is, therefore, necessary to protect the C^2MOS IC from the external electric stress, such as the discharge from ambient charged body, the induction from space electric field, etc.

Therefore, in transporting and storing C^2MOS IC, it is necessary to use the conductive mat, metallic box, the box lined with aluminum foil, etc. so that each terminal of IC may become the same electric potential.

TOSHIBA C^2MOS IC is inserted in the conductive case or conductive mat at the time of shipment. Therefore, IC should not be removed from the case or mat with the exception of the case where the removal is required. In particular, refrain from using plastic cases or vinyl bags on which static electricity is liable to be generated.

Store the IC at the location where it is not exposed to the direct sunlight. Pay careful attention to store at the location of the relative humidity which should be neither extremely high not extremely low.

2.2 Acceptance inspection

In case of conducting acceptance test on C^2MOS IC, first of all it is necessary to ascertain that there is no transient phenomenon as overshoot or undershoot etc. between each terminal of test system by using synchroscope. Next, conduct test by using the calibration IC for ascertaining that there is no error in the test program. In the case of giving test pulses, it is necessary to give input signal after turning on the power supply.

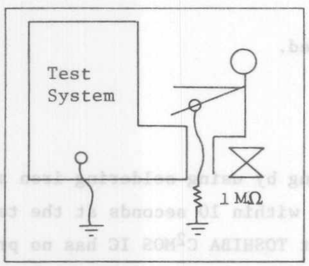


Fig. 4 Grounding

t is necessary to take out the IC on the grounded work table. In conducting the test, ground the test system and inspector. For preventing the electric shock accident by the electricity leak from electric equipment, ground the inspector through approx. 1MΩ resistor without fail.

Be sure to turn off the power supply when IC is inserted in IC socket or IC is drawn out of the socket. The accident of test system may give fatal damage to IC. It is, therefore, advisable to carry out the self-diagnosic program in advance before test.

2.3 Assembling

As mentioned in 2.2, in case of installing C^2MOS IC on the printed base board, it is necessary to make protection from the static electricity by grounding electric equipment, work tables (desks), and work men. It is advisable to ground a work table by putting metal plate or aluminum foil on the surface. Refrain as practicable as possible from wearing chemical fiber work cloth. Electricity leak from electric equipment shall be prevented by reason of safety. So, it is necessary to periodically check to see that there is no leak in the electric equipment.

In case of shaping the lead frame for installing IC,it is recommended that pincette and other jigs be used for preventing the stress from being imposed on the root.
It is ideal that the jigs are grounded.

2.4 Soldering and cleaning

In case of carrying out soldering by using soldering iron and soldering tank, perform the soldering work within 10 seconds at the temperature 260°C below. It is confirmed that TOSHIBA C^2MOS IC has no problem on reliability even in case the temperature stress is given to the stopper of lead at 260°C for 10 seconds.

Use the soldering iron with no leak on its tip. It is advisable to use A class soldering iron, the dielectric resistance of which is over 10 MΩ.

In using the soldering tank, it is necessary to ground the tank for preventing the unstable electric potential. After soldering IC to a printed base board, for removing flux and others, accelerating cleaning method is adopted in many cases by using detergent and ultrasonic wave.

In this case, full attention should be given to the selection of solvent so that the cleaning may have no influence on the outer case and mark of C^2MOS IC. In general, it is advisable to use FUREON series detergent, FUREON TE, and DAIFURON solvent S3-E. In the ultrasonic cleaning, consideration should be given to the cleaning method so that the main body may form a shadow to the oscillator. This is for preventing IC and base board from the stress by resonance. At the same time, consideration should be given to the cleaning time which shall be within 30 seconds.

2.5 Adjustment and test

In conducting adjustment and test of set on completion of printed base board, before turning on the power supply it is advisable to ascertain that there are no errors in polarity and others of power supply, etc. As to the printed base board, ascertain that there are no solder bridge, cracks, etc. Usually, the C^2MOS system requires only a small supply current, so that the abnormality of system can be checked, from the excessive supply current. In case of conducting test by using the commercially available constant-voltage power supply, it is recommended that the current limit be imposed on the power supply.

For the system consisting of several sheets of printed base boards, the printed base boards should be drawn out of and insert in the mother board for checking the system. In this case, the work shall be made after turning off the power supply.

In observing each part of printed base board with an oscilloscope at the time of test, it is necessary to be careful so that the tip of probe may not contact other signal wires and supply wire. In case the location to be observed is decided in advance, it is one of the methods to stand the test pin for exclusive use. Do not lead out this test pin directly from the signal wire. It is advisable to protect C^2MOS circuit from static electricity and erroneous connection by inserting over 10KΩ resistance in series.

In case of conducting test at high temperature and low temperature, it is necessary to ground the thermostatic oven. The set in the oven should be installed on the conductors.

3. Cautions on Designing Circuits

3.1 Input processing

As the input of CMOS IC is very high impedance ($R_{IN} \doteqdot 10^{12}\Omega$), the logic level is not constant in the open state. In this case, if the input is in the medium level, both P-channel and N-channel transistors are in the state of connection, whereby the unnecessary supply current flows.

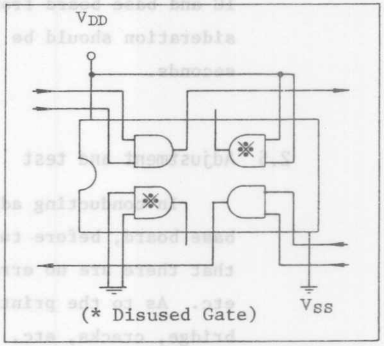


Fig.5 Example of Input Processing

Therefore, be sure to connect the unnecessary input line to V_{DD}, V_{SS} or other input/output wires, for which logic level is decided, as shown in Fig. 5. Unstable contact of soldered parts causes erroneous working of CMOS system or increase in supply current. Therefore, care should be taken to wiring.

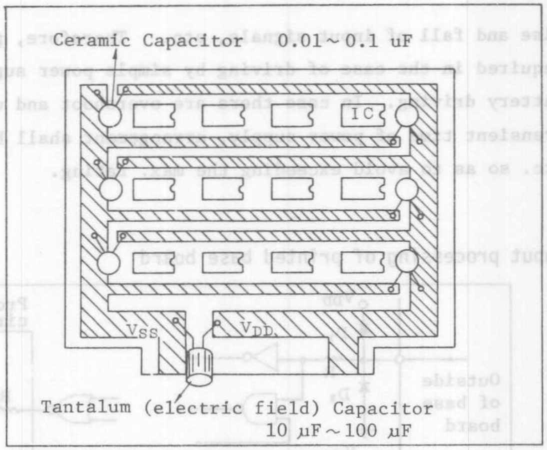


Fig. 6 Example of Printed Base Board

3.2 Designing power supply

In general, CMOS is small in current consumption as compared with other bipolar digital IC ; therefore, it can be used by the small capacity power supply. By reason of its operation, however, CMOS consumes electric power in the form of spike. This makes it necessary to make the high-frequency impedance of power supply lower. Concretely speaking, it is necessary to make supply (V_{DD}) wire and GND (V_{SS}) wire thick and short and insert 0.01 μF ~ 0.1μF capacitors as the high-frequency filters in the inportant areas between power supply and GND on the printed base board. As to the low-frequency filter. 10 μF ~ 100 μF/printed base baord will do for the purpose. Fig. 6 shows an example of printed base boards.

And average supply current varies considerably depending on such factors as the working frequency, load on capacitor, supply voltage,

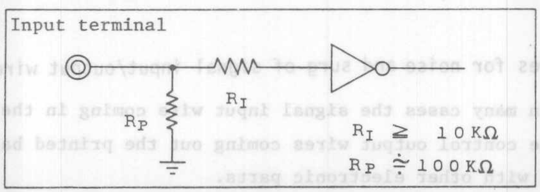
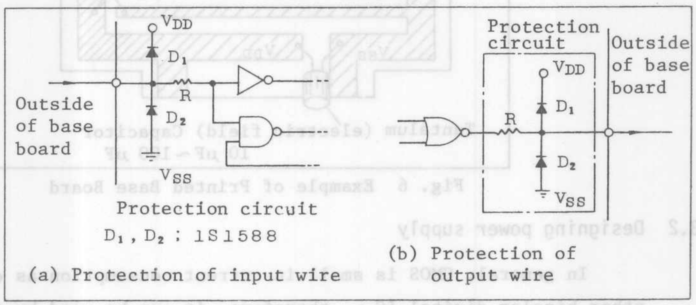


Fig. 7 Input Processing of Printed Base Board

rise and fall of input signals, etc. Therefore, particular attention is required in the case of driving by simple power supply of Zenor diode of battery driving. In case there are overshoot and undershoot at the transient time of power supply, arrangement shall be made by using filters, etc. so as to avoid exceeding the max. rating.

3.3 Input processing of printed base board



(a) Protection of input wire

(b) Protection of output wire

Fig. 8 Protection of Input/Output Wires

When the input terminal of printed base board consists of C^2MOS input only, like the individual CMOS device, the input terminal is in electrically floating condition, whereby there is a possibility of receiving damage by static electricity, etc. Therefore, as shown in Fig. 7, by inserting over 10 KΩ resistance in series in advance, it is possible to protect C^2MOS from the overcurrent.

And, it is more effective if the input terminal can be pulled up or down by approx 100 KΩ resistance.

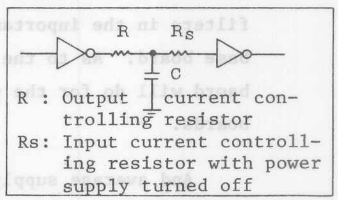


Fig.9 Method of Inserting Capacitor

3.4 Measures for noise and surg of signal input/output wire

In many cases the signal input wire coming in the printed base board and the control output wires coming out the printed base board are connected with other electronic parts.

In general, it can be said that the signal wire is long in many cases. In case the surge is applied to these input/output wires by induction, there is a possibility of deterioration or breakdown of CMOS IC being caused by overcurrent (overvoltage). Therefore, in case the input/output signal wires are long and when the high voltage wire exists in the outside printed base board, it is necessary to insert the protective circuit as shown in Fig. 8. The method of separating the base board through photocoupler and lead relay contact is also effective.

In case of making test pin, it is advisable to make protection in advance as shown in Fig. 5 to Fig. 8.

3.5 Signal wire and capacitor to be connected to V_{DD} or V_{SS}

In case the capacitor is connected directly to signal wire for removing the delay and noise in signal, the capacitor up to 500pF in capacity can be connected directly, but capacitors larger in capacity shall be connected through such resistors as shown in Fig. 9. These resistors are used for restricting the flow of current to the parasitic circuit of CMOS input/output at the time of "ON" and "OFF" of power supply and for preventing CMOS output from short-circuiting for a long time. It can be said that 10 KΩ or over will be suitable as the resistance value for both R and R_S.

3.6 Output short-circuiting

In C^2MOS IC, buffer is added to the output, whereby it is possible to carry out the current driving of both sorse (I_{OH}) and sink (I_{OL}). Therefore, in case "H" level output wire is short-circuited with GND (V_{SS}) wire or "L" level output wire is short-circuited with V_{DD} wire, overcurrent flows to C^2MOS output. In particular, if supply voltage is high, this current may cause the package to exceed the permissible power disipation; therefore, attention shall be given to prevention of the output short-circuit.

Of course, it is impossible to connect normal outputs together, but concerning the C^2MOS which has three-state output, wired OR is permitted under the condition that more than two-wire outputs do not come to enable simultaneously.

3.7 Influence of input slow in rise or fall time

In case the waveform slow in rise time or fall time is applied to CMOS input, the output of gate IC,etc. may tend to oscillate in the neighborhood of V_{TH} (device threshold Voltage) of input waveform. This is because, in the neighborhood of V_{TH}, CMOS gate becomes equivalently linear amplification, whereby the minute supply ripples and noise appear on the output after amplification.

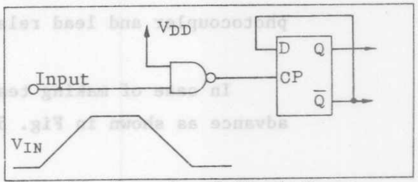


Fig. 10 Example of Clock Input Shaped by Waveform

For suppressing the above phenomenon, consideration should be taken to insert the high-frequency filter capacitor between V_{DD} and V_{SS} of oscillating IC or to use Schmitt trigger IC. In particular, attention should be given to the clock input of sequence circuit. Fig. 10 shows an example of clock shaping.

3.8 Variation of various characteristics

(a) Circuit threshold voltage

The circuit threshold voltage of C^2MOS is designed for 1/2 V_{DD} ideally, but in reality the voltage is influenced directly by the variations of both P/N FETs because the voltage is decided by the voltage dividing effect of both P/N MOS FETs. As compared with the bipolar IC, therefore, the variation is considerably large. For example, differentiation circuit/integration circuit by CR and timer circuit are greatly influenced in terms of time by this variation, and in reality compensation effect is required by the use of variable resistors.

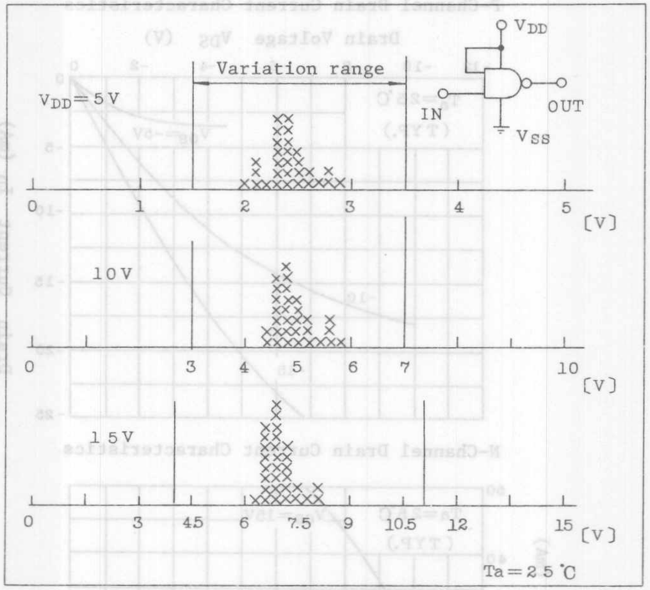


Fig. 11 Variation Data of TC4011BP V_{TH}

Fig. 11 shows the variation data for TC4011BP circuit threshold voltage. As to other types, variations can be considered to be similar to TC4011BP.

(b) Output current

The variation of output current can be considered to be Max. ±30% to the standard value. Fig. 12 shows the output current characteristics (standard value) of TC4007UBP. So far as this figure is concerned, it follows that considerable drain current flow at the domain where V_{DD} is high. However, if output current is large,internal loss of FET becomes large at the same time, resulting in lowering the thermal reliability. In reality, therefore, it is suitable to use at the non-saturation domain up to $|V_{DS}| < 1.5V$.

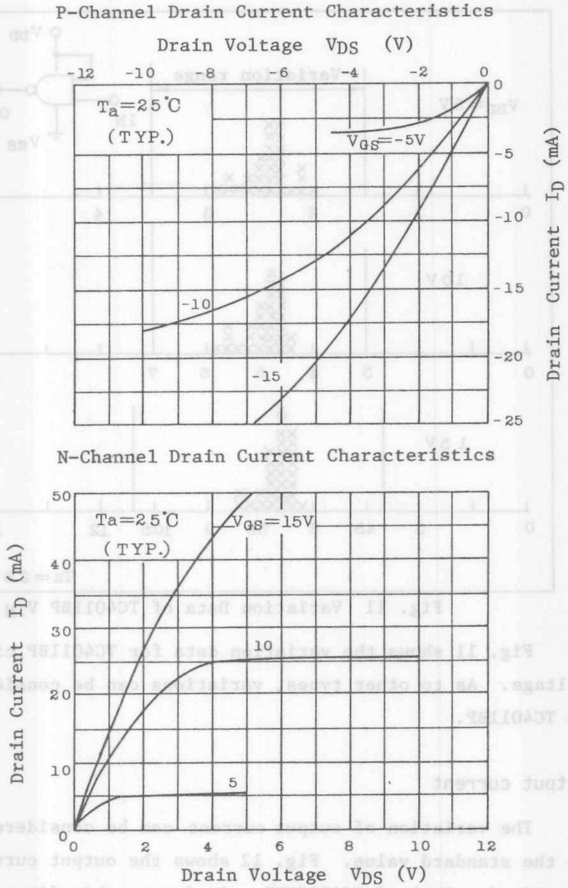


Fig. 5-12 Output Current Characteristics of TC4007UBP

(c) Switching time

Propagation times such as t_{PLH}, t_{PHL}, etc., toggle frequency of counter, etc. have max. ±30% variation to the standard value.

However, these parameters vary depending on the interface conditions of load capacitance, etc., therefore, it is necessary to consider fanout at the portion where operating speed is high.

3.9 Temperature parameters of various characteristics

(a) Device threshold voltage

The device threshold voltage is considerably stable to the temperature because the temperature coefficients of ON resistance of P-channel and N-channel FETs become the plus values. The temperature coefficients are approx. $-2 \sim -3$ mV/°C at V_{DD} = 5V and approx. $-4 \sim -5$ mV/°C at V_{DD}=10V.

(b) Output current

The output current has the minus temperature coefficients for both P/N FETs, which are approx.-0 4%/°C. Namely, under the temperature condition of approx. 85°C the current value becomes small by about 25% as compared with the normal temperature (about 25°C). This is an important point in deciding the overdrive coefficient in case of driving transistor, etc. by current.

(c) Input current, static current consumption, and output 3-state leak current

These leak currents are theoretically the leak currents in the opposite direction of PN junction, and are extremely small in value at normal temperature. With the rise in temperature, however, the values increase at exponential function.

In reality, it is convenient to remember that with the rise in ambient temperature by 25°C the leak current increases by about 1 digit.

However, in reality the input current is approx. $10^{-10} \sim 10^{-11}$ [A] at normal temperature and the static current consumption is approx. 10^{-9} [A] at gate IC. These are the levels which have no problems on the practical use at high temperature.

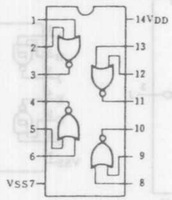
(d) Propagation time and max. frequency

As the propagation time may be regarded as the time for charging and discharging the internal capacitance and load capacitance of ON resistance of FET, the propagation time is considered to be equivalent to the temperature coefficient of ON resistance. Therefore, the temperature coefficient becomes approx. 0.4%/°C, while, in the neighborhood of 85°C, t_{PLH} and t_{PHL} increase by approx. 25% to the normal temperature value. On the contrary, the max. frequency decreases by approx. 25%.

〔5〕 BLOCK DIAGRAM/PINCONFIGURATION

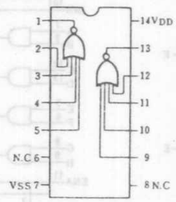
Pin Connection

TC4001BP/UBP



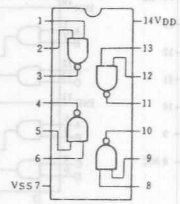
QUAD 2-INPUT POSITIVE NOR GATE
PACKAGE;5-21F

TC4002BP



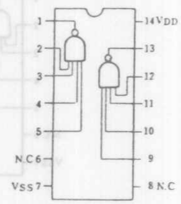
DUAL 4-INPUT POSITIVE NOR GATE
PACKAGE;5-21F

TC4011BP/UBP



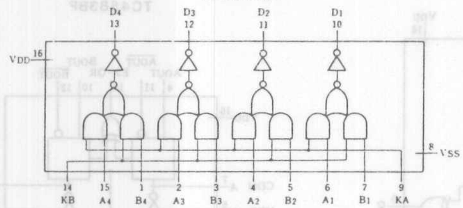
QUAD 2-INPUT POSITIVE NAND GATE
PACKAGE;5-21F

TC4012BP



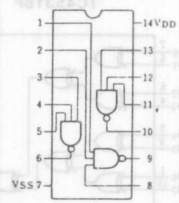
DUAL 4-INPUT POSITIVE NAND GATE
PACKAGE;5-21F

TC4019BP



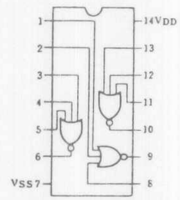
QUAD AND OR SELECT GATE
PACKAGE;5-22E

TC4023BP



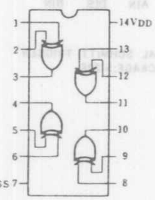
TRIPLE 3-INPUT POSITIVE NAND GATE
PACKAGE;5-21F

TC4025BP



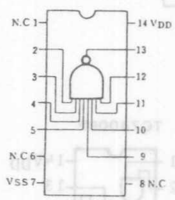
TRIPLE 3-INPUT POSITIVE NOR GATE
PACKAGE;5-21F

TC4030BP



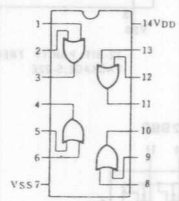
QUAD EXCLUSIVE-OR GATE
PACKAGE;5-21F

TC4068BP



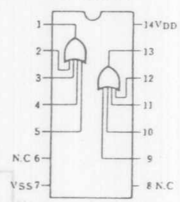
8-INPUT POSITIVE NAND GATE
PACKAGE;5-21F

TC4071BP



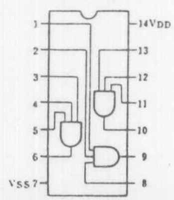
QUAD 2-INPUT POSITIVE OR GATE
PACKAGE;5-21F

TC4072BP



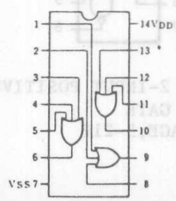
DUAL 4-INPUT POSITIVE OR GATE
PACKAGE;5-21F

TC4073BP



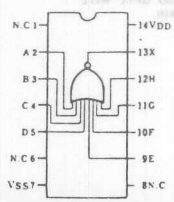
TRIPLE 3-INPUT POSITIVE AND GATE
PACKAGE;5-21F

TC4075BP



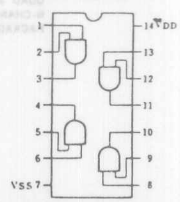
TRIPLE 3-INPUT POSITIVE OR GATE
PACKAGE;5-21F

TC4078BP



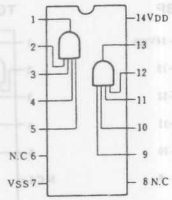
8-INPUT POSITIVE NOR GATE
PACKAGE;5-21F

TC4081BP



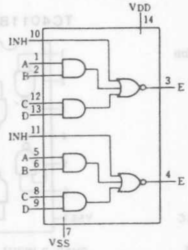
QUAD 2-INPUT POSITIVE AND GATE
PACKAGE;5-21F

TC4082BP



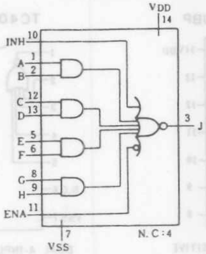
DUAL 4-INPUT POSITIVE AND GATE
PACKAGE;5-21F

TC4085BP



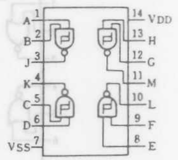
DUAL AND OR INVERT GATE
PACKAGE;5-21F

TC4086BP



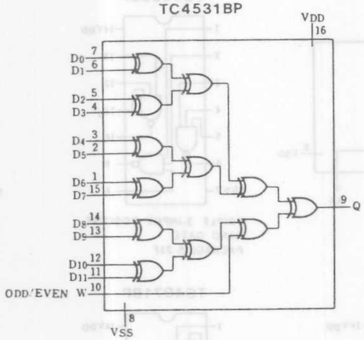
AND OR INVERT GATE
PACKAGE;5-21F

TC4093BP



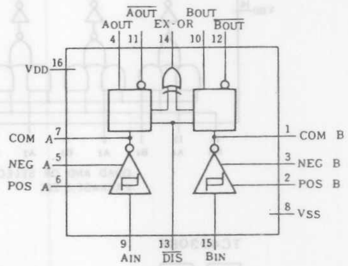
QUAD 2-INPUT NAND SCHMITT TRIGGER
PACKAGE;5-21F

TC4531BP



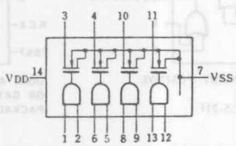
12-BIT PARITY TREE
PACKAGE;5-22E

TC4583BP



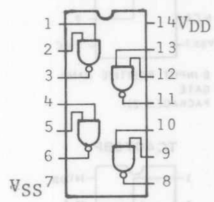
DUAL SCHMITT TRIGGER
PACKAGE;5-22E

TC5029BP



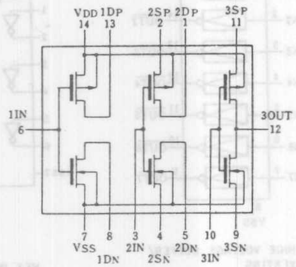
QUAD 2-INPUT NAND GATE WITE N-CHAN OPEN DRAIN
PACKAGE;5-21F

TC7400BP



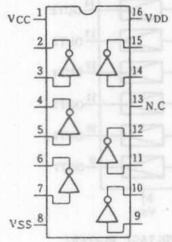
QUAD 2-INPUT POSITIVE NAND GATE
PACKAGE;5-21F

TC4007UBP



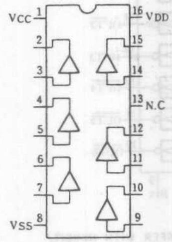
DUAL COMPLEMENTARY PAIR PLUS INVERTER
PACKAGE;5-21F

TC4009UBP



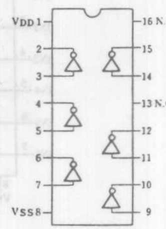
HEX INVERTING BUFFER/
CONVERTER
PACKAGE;5-22E

TC4010BP



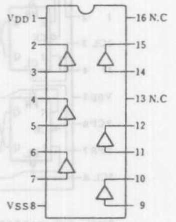
HEX NON-INVERTING BUFFER/
CONVERTER
PACKAGE;5-22E

TC4049BP



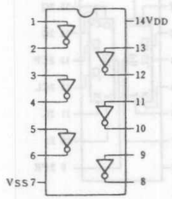
HEX INVERTING BUFFER/
CONVERTER
PACKAGE;5-22E

TC4050BP



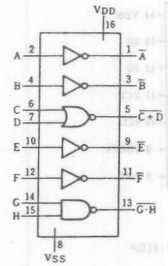
HEX NON-INVERTING
BUFFER CONVERTER
PACKAGE;5-22E

TC4069UBP



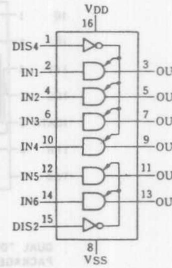
HEX INVERTER
PACKAGE;5-21F

TC4572BP



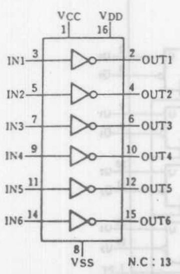
HEX GATE 4-INVERTER PLUS
2-INPUT NOR GATE PLUS
2 -INPUT NAND GATE
PACKAGE;5-22E

TC5012BP



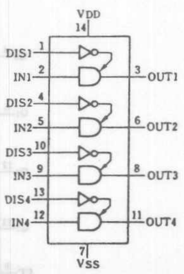
3-STATE NON-INVERTING
BUFFER
PACKAGE;5-22E

TC5020BP



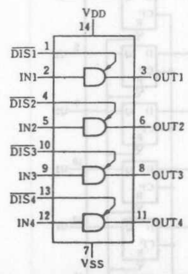
HEX LOW TO HIGH VOLTAGE
TRANSLATOR
PACKAGE;5-22E

TC5024BP



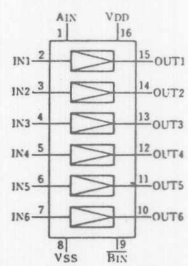
QUAD 3-STATE BUS
BUFFER ("L"LEVEL)
PACKAGE; 5-21F

TC5025BP



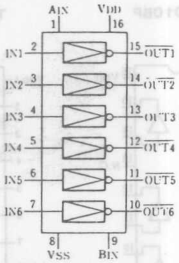
QUAD 3-STATE BUS
BUFFER ("H"LEVEL)
PACKAGE;5-21F

TC5064BP



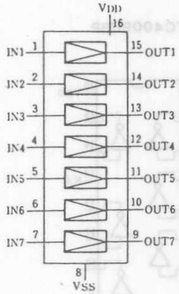
HEX HIGH VOLTAGE BUFFER WITH INHIBIT/
NON INVERTING
PACKAGE;5-22E

TC5065BP



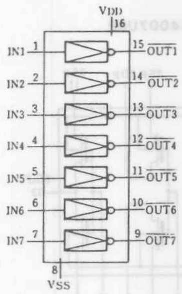
HEX HIGH VOLTAGE BUFFER WITH INHIBIT/
INVERTING
PACKAGE;5-22E

TC5066BP



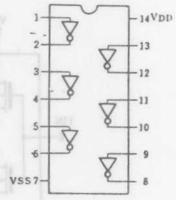
7-HIGH VOLTAGE BUFFER/
NON INVERTING
PACKAGE;5-22E

TC5067BP



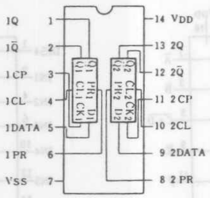
7-HIGE VOLTAGE BUFFER/
INVERTING
PACKAGE;5-22E

TC7404UBP



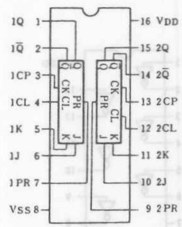
HEX INVERTER
PACKAGE5-21F

TC4013BP



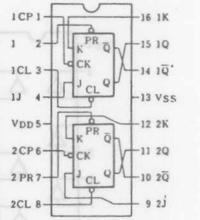
DUAL "D"TYPE FLIP FLOP
PACKAGE;5-21F

TC4027BP



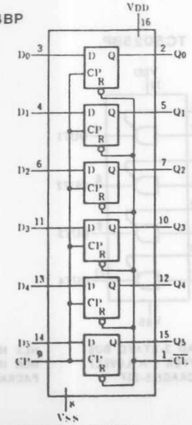
DUAL J/K MASTER-SLAVE
FLIP FLOP
PACKAGE;5-22E

TC7476BP



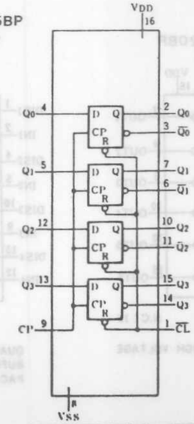
DUAL J/K MASTER-SLAVE
FLIP FLOP
PACKAGE;5-22E

TC40174BP



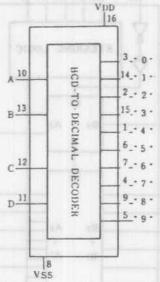
HEX TYPE D FLIP FLOP
PACKAGE 5-22E

TC40175BP



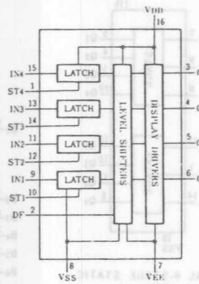
QUAD TYPE D FLIP FLOP
PACKAGE;5-22E

TC4028BP



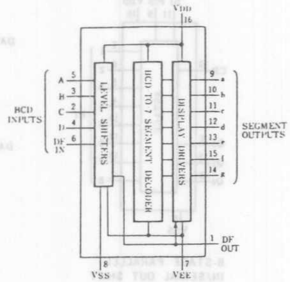
BCD-TO-DECIMAL DECODER
PACKAGE;5-22E

TC4054BP



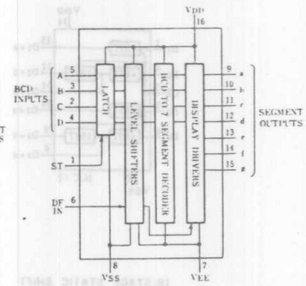
4-SEGMENT LC DISPLAY DRIVER
PACKAGE;5-22E

TC4055BP



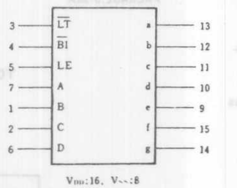
BCD TO 7-SEGMENT DECODER/
LC DISPLAY DRIVER
PACKAGE;5-22E

TC4056BP



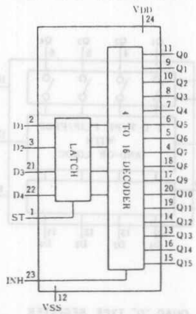
BCD TO 7-SEGMENT DECODER/
LC DISPLAY DRIVER
PACKAGE;5-22E

TC4511BP



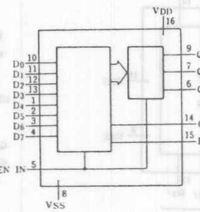
7-SEGMENT LATCH/DECODER/DRIVER
PACKAGE;5-22E

TC4514BP/TC4515BP



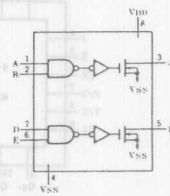
4-BIT LATCH/4-TO-16 LINE
DECODER
PACKAGE;5-22E

TC4532BP



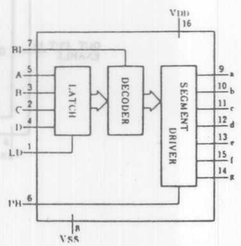
8-BIT PRIORITY ENCODER
PACKAGE;5-32A

TC40107BP



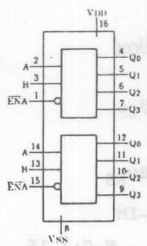
DUAL 2-INPUT NAND
BUFFER/DRIVER
PACKAGE; 5-10

TC4543BP



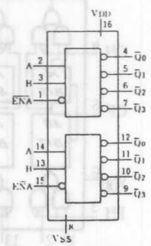
BCD TO 7-SEGMENT LATCH/DECODER/
DRIVER
PACKAGE;5-22E

TC4555BP



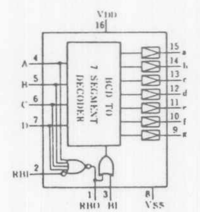
DUAL 1 OF 4 DECODER
(POSITIVE)
PACKAGE;5-22E

TC4556BP



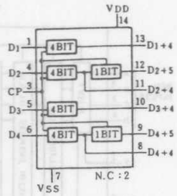
DUAL 1 OF 4 DECODER
(NEGATIVE)
PACKAGE;5-22E

TC5002BP/TC5022BP



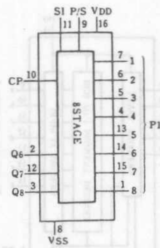
BCD TO 7-SEGMENT DECODER/
DRIVER
PACKAGE;5-22E

TC4006BP



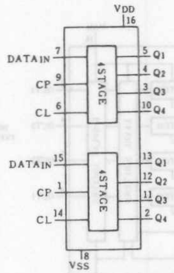
18-STAGE STATIC SHIFT REGISTER
PACKAGE;5-21F

TC4014BP/TC4021BP



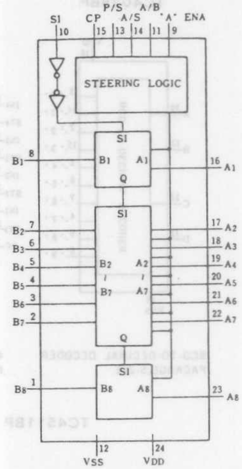
8-STAGE PARALLEL IN/SERIAL OUT SHIFT REGISTER
PACKAGE;5-22E

TC4015BP



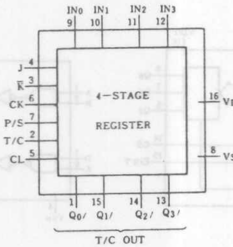
DUAL 4-STAGE STATIC SHIFT REGISTER
PACKAGE;5-22E

TC4034BP



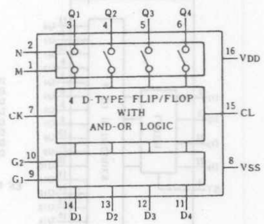
8-BIT BIDIRECTIONAL BUS REGISTER
PACKAGE;5-32A

TC4035BP



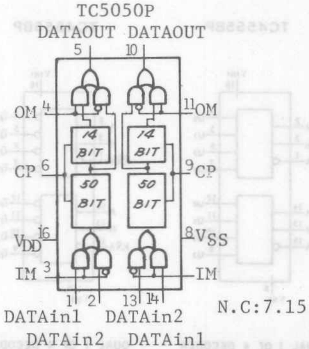
4-BIT PARALLEL IN PARALLEL OUT SHIFT REGISTER
PACKAGE;5-22E

TC4076BP



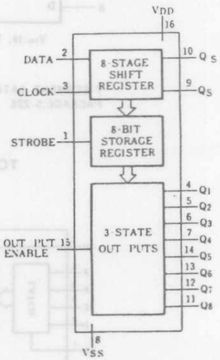
QUAD "D" TYPE REGISTER
PACKAGE;5-22E

TC5050P



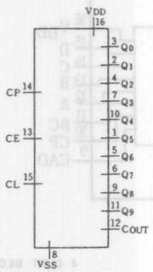
DUAL 50/64-BIT STATIC SHIFT REGISTER
PACKAGE;5-22E

TC4094BP



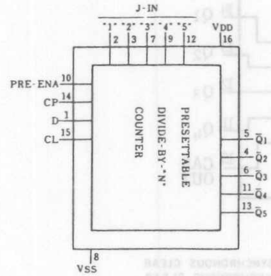
8-STAGE SHIFT-AND-STORE BUS REGISTER
PACKAGE;5-22E

TC4017BP



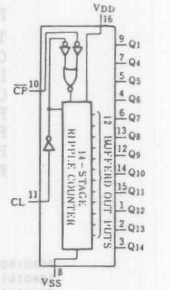
DECADE COUNTER/
DIVIDER
PACKAGE;5-22E

TC4018BP



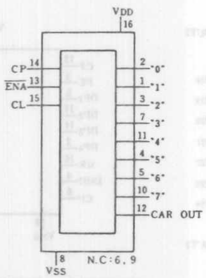
PROGRAMMABLE DIVIDE BY N-COUNTER
PACKAGE;5-22E

TC4020BP



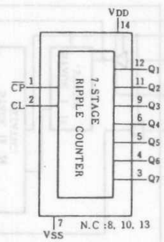
14-STAGE BINARY COUNTER
PACKAGE;5-22E

TC4022BP



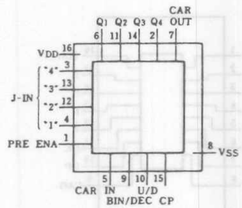
DIVIDE BY 8-COUNTER/DIVIDER
PACKAGE;5-22E

TC4024BP



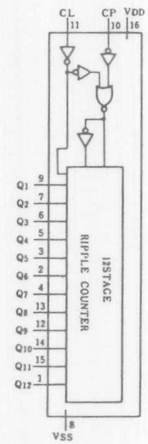
7-STAGE BINARY COUNTER
PACKAGE;5-21F

TC4029BP



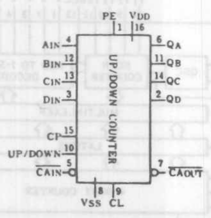
PRESETTABLE UP/DOWN COUNTER
PACKAGE;5-22E

TC4040BP



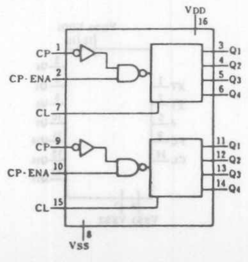
12-STAGE BINARY
COUNTER
PACKAGE;5-22E

TC4510BP/TC4516BP



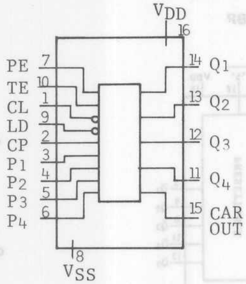
TC4510BP; BCD UP/DOWN COUNTER
TC4516BP; BINARY UP/DOWN COUNTER
PACKAGE;5-22E

TC4518BP/TC4520BP



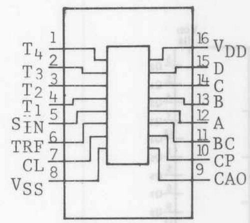
DUAL BCD UP COUNTER/DUAL BINARY
UP COUNTER
PACKAGE;5-22E

TC40160BP/TC40161BP
TC40162BP/TC40163BP



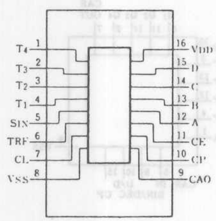
TC40160BP/ DECADE WITH ASYNCHRONOUS CLEAR
TC40161BP/ BINARY WITH ASYNCHRONOUS CLEAR
TC40162BP/ DECADE WITH SYNCHRONOUS CLEAR
TC40163BP/ BINARY WITH SYNCHRONOUS CLEAR
PACKAGE;5-22E

TC5051P



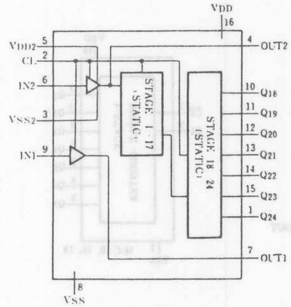
4 DIGIT DECADE COUNTER WITH/
BLANKING CONTROL
PACKAGE;5-22E

TC5052P



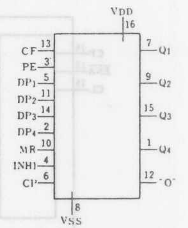
4 DIGIT DECADE COUNTER WITH/
CLOCK ENABLE
PACKAGE;5-22E

TC4521BP



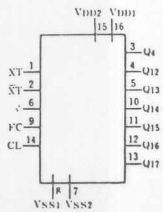
24-STAGE FREQUENCY DIVIDER
PACKAGE;5-22E

TC4522BP
TC4526BP



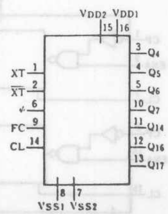
TC4522BP/PROGRAMMABLE DIVIDE BY N
4-BIT BCD COUNTER
TC4526BP/PROGRAMMABLE DIVIDE BY N
4-BIT BINARY COUNTER
PACKAGE;5-22E

TC5036P



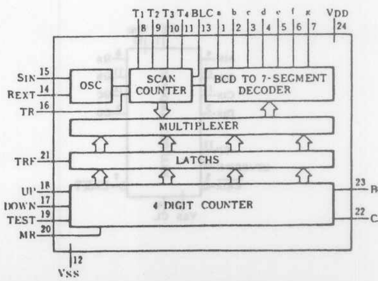
17-STAGE HIGH SPEED FREQUENCY DIVIDER
PACKAGE;5-22E

TC5048P



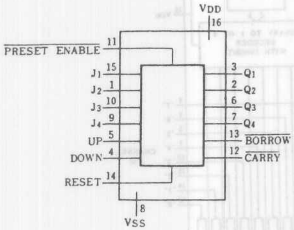
17-STAGE HIGH SPEED FREQUENCY DIVIDER
PACKAGE;5-22E

TC5053P
TC5054P



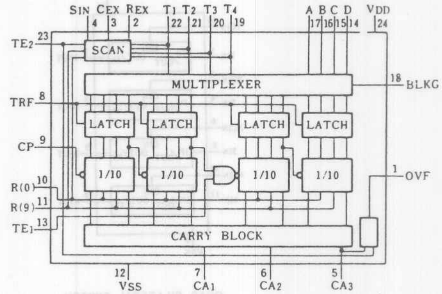
4-DIGIT UP/DOWN COUNTER
PACKAGE;5-32A

TC40192BP/193BP



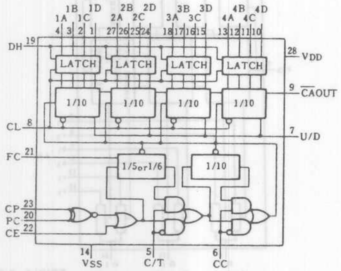
TC40192BP; PRESETTABLE U/D BCD COUNTER
TC40193BP; PRESETTABLE U/D 4-BIT BINARY COUNTER
PACKAGE; 5-22E

TC5001P



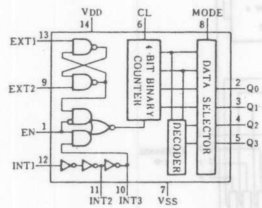
4-DIGIT DECADE COUNTER
PACKAGE; 5-32A

TC5010P



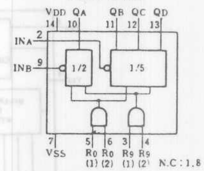
4-DIGIT UP/DOWN COUNTER WITH TIMER
PACKAGE; 5-37

TC5018P



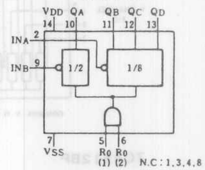
4-STAGE BINARY COUNTER WITE RC OSC.
PACKAGE; 5-21F

TC5026BP



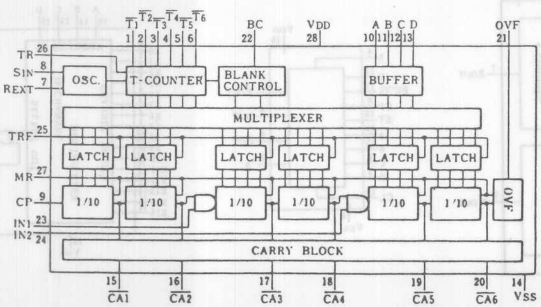
BCD UP COUNTER
PACKAGE; 5-21F

TC5027BP



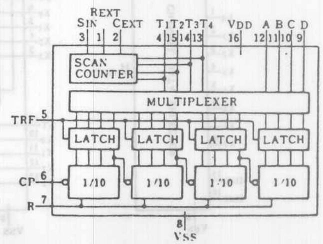
BINARY UP COUNTER
PACKAGE; 5-21F

TC5032P



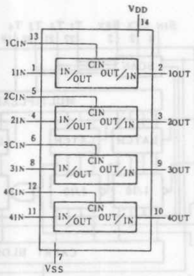
6-DIGIT DECADE COUNTER
PACKAGE; 5-37

TC5037P



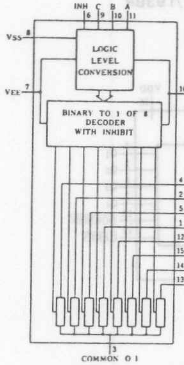
4-DIGIT DECADE COUNTER
PACKAGE; 5-22E

TC4016BP/TC4066BP



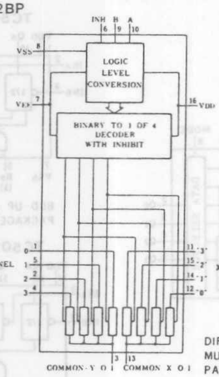
QUAD BILATERAL SWITCH
PACKAGE 5-21F

TC4051BP



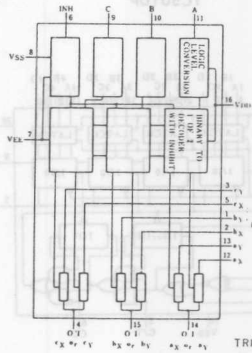
SINGLE 8-CHANNEL ANALOG MULTIPLEXER DEMULTIPLEXER
PACKAGE;5-22E

TC4052BP



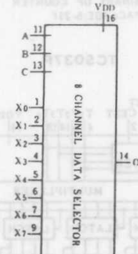
DIFFREENTJAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
PACKAGE;5-22E

TC4053BP



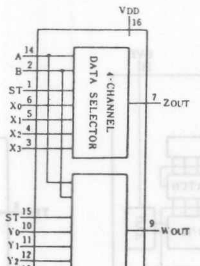
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER
PACKAGE;5-22E

TC4512BP



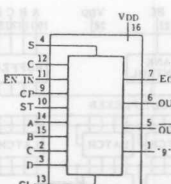
8-CHANNEL DATA SELECTOR
PACKAGE;5-22E

TC4539BP



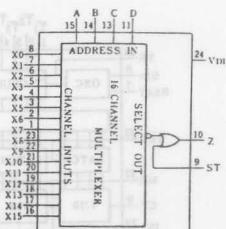
DUAL 4-CHANNEL MULTIPLEXER
PACKAGE;5-22E

TC4527BP



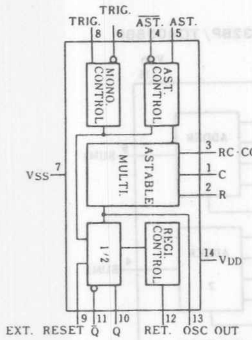
BCD RATE MULTIPLIER
PACKAGE;5-22E

TC5023BP



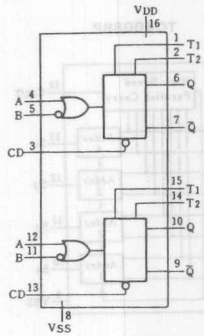
16-CHANNEL MULTIPLEXER
PACKAGE;5-32A

TC4047BP



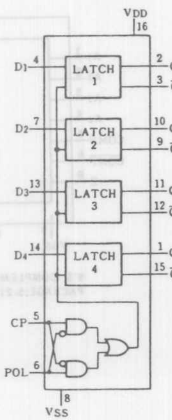
ASTABLE/MONOSTABLE MULTIVIBRATOR
PACKAGE;5-21F

TC4528BP



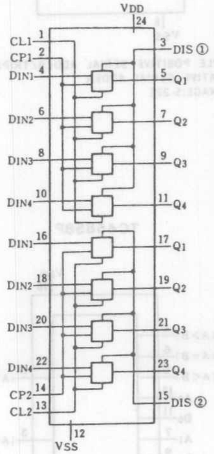
DUAL MONOSTABLE
MULTIVIBRATOR
PACKAGE;5-22E

TC4042BP



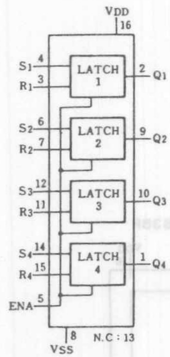
QUAD "D" LATCH
PACKAGE;5-22E

TC4508BP



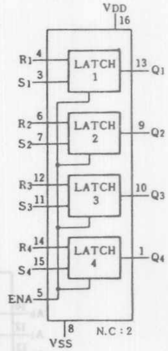
DUAL 4-BIT LATCH
PACKAGE;5-32A

TC4043BP



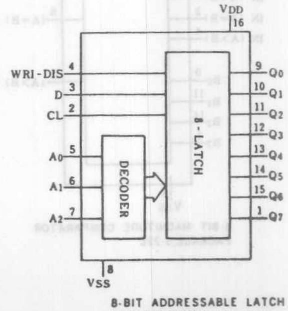
QUAD POSITIVE NOR
R/S LATCH
PACKAGE;5-22E

TC4044BP



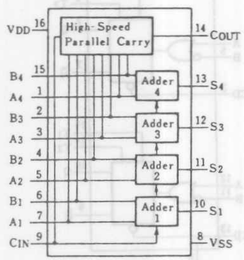
QUAD POSITIVE NAND
R/S LATCH
PACKAGE;5-22E

TC4099BP



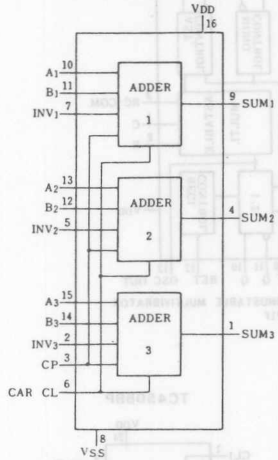
8-BIT ADDRESSABLE LATCH
PACKAGE;5-22E

TC4008BP



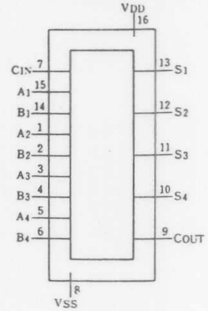
4-BIT FULL ADDER
PACKAGE;5-22E

TC4032BP/TC4038BP



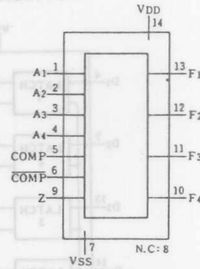
TRIPLE POSITIVE SERIAL ADDER/TRIPLE
NEGATIVE SERIAL ADDER
PACKAGE;5-22E

TC4560BP



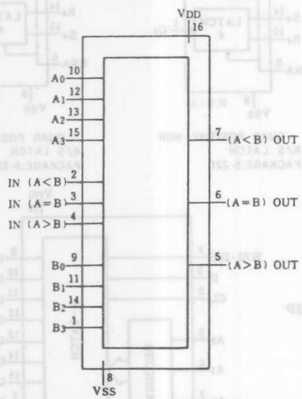
N BCD ADDER
PACKAGE;5-22E

TC4561BP



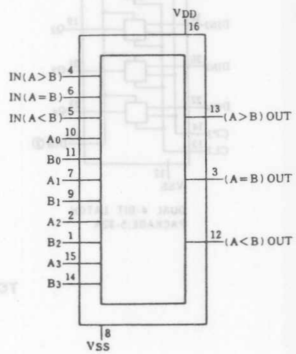
9'S COMPLEMENTER
PACKAGE;5-21F

TC4063BP



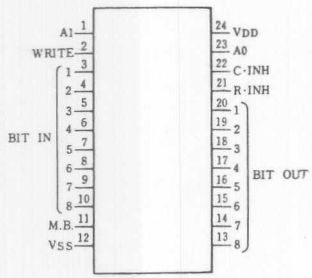
4-BIT MAGNITUDE COMPARATOR
PACKAGE;5-22E

TC4585BP



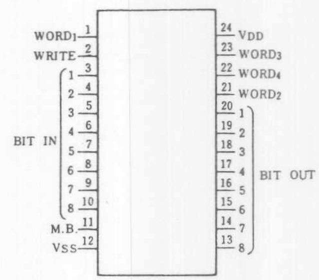
4-BIT MAGNITUDE COMPARATOR
PACKAGE;5-22E

TC4036BP



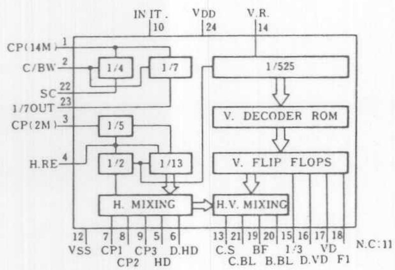
4 WORD × 8 BIT STATIC RAM
(BINRY ADDRESSING)
PAKRAGE;5-32A

TC4039BP



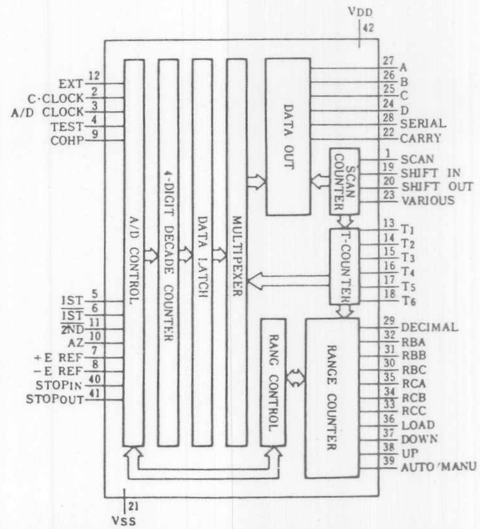
4 WORD × 8BIT STATIC RAM
(DIRECT WORD-LINE ADDRESSING)
PAKRAGE;5-32A

TC5003P



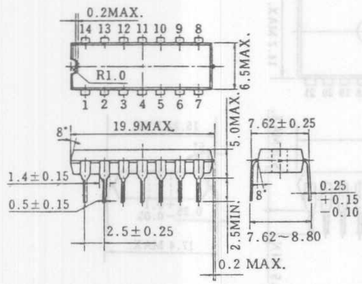
TV SYNC GENERATOR
PACKAGE;5-32A

TC5055P

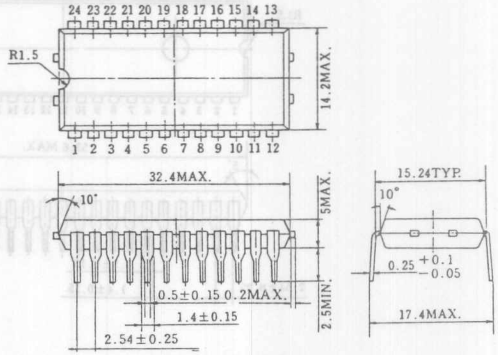


$3\frac{1}{2}$ DIGIT DVM CIRCUIT
PACKAGE;5-54

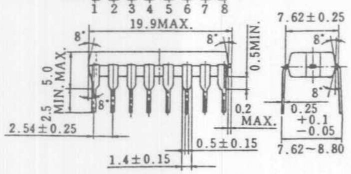
〔6〕 PACKAGE



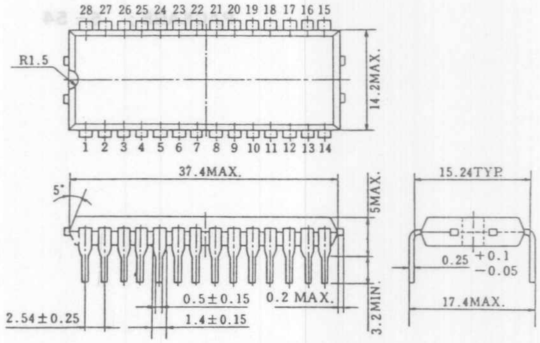
PACKAGE ; 5-21F



PACKAGE ; 5-32A

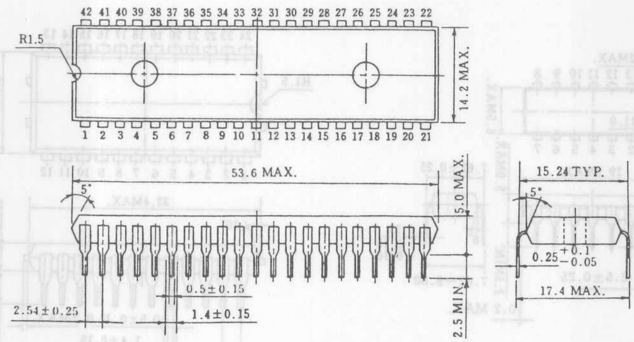


PACKAGE ; 5-22E



PACKAGE ; 5-37

External Dimension



PACKAGE ; 5−54